



QSFP28

EQ231M10X-3LCD10

100G and 112G QSFP28 LR4 10KM Optical Transceiver

- Compliant with the QSFP28 MSA Technical Specifications
- Supports 103.1Gb/s and 112Gb/s data rates
- Maximum link length of 10km on Single Mode Fiber (SMF)
- Optical specifications are compliant with IEEE802.3ba 100GBASE-LR4 and OTU4 4I1-9D1F requirements specified in ITU-T
- Low speed electrical signal is compliant with SFF-8679
- ➤ High speed electrical signal is compliant with 802.3bm CAUI-4
- Digital diagnostic functions are available via the I2C interface, as specified by SFF-8636
- ➤ 4x28Gb/s DFB-based LAN-WDM transmitter with central wavelengths of 4 channels 1295.56, 1300.05, 1304.58 and 1309.14 nm.
- Supports operation for a case temperature of 0°C to +70 °C
- Duplex LC receptacles
- ➤ Power Dissipation < 4.5W
- Single 3.3V Power Supply
- > ROHS Compliant



Applications

- > 100GBASE-LR4 Ethernet links
- ➢ OTN OTU4 4I1-9D1F

Description

The ETU QSFP28 LR4 is a 4x28G single-mode fiber, hot pluggable optical transceiver. ETU's unique SystemOnGlassTM (SOGTM) technology enables the integration of 4 transmitters, 4 receivers and an optical MUX/ DeMUX into a small form factor package that delivers up to 112 Gbps data link in a compact QSFP28 footprint.

The optical connectivity is based on two Singlemode Fiber (SMF) LC connectors, one for Tx and one for Rx. The Tx and Rx each consist of 4 28GB/s LAN-WDM channels, whose wavelengths are in the 1300nm range. The QSFP28 LR4 transceiver is designed for applications with a reach up to 10Km.

The ETU QSFP28 transceiver is based on proprietary ETU PLC technology, using surface mounted opto-electronic devices with no free space elements. The unique design of the optical engine facilitates unparalleled compactness while maintaining Telcordia robustness.

Absolute Maximum Ratings

Parameter	Symb	Min	Max	Unit	Notes	
	ol					
Storage Temperature Range	T_{STG}	-40	+85	°C		
Supply Voltage	V_{CC}	0	4	V		
Maximum Average Input Optical	P _{IN}	5.5		dBm		
Power per Lane (Damage Threshold)						
Relative Humidity	RH	10% to 90%				
		non-condensing				

Operating Conditions

Parameter	Symb	Min	Max	Unit	Notes
	ol				
Case Temperature- Operating	T _{CASE}	0	70	°C	
Supply Voltage	Vcc	3.14	3.46	٧	
Power Consumption	P _{DISS}		3.5	W	
Power Consumption- LP Mode	P _{DISS-LP}		1.5	W	

100GBASE-LR4 Operation

Transmitter Parameter	Lane	Min	Typica	Max	Unit	Note
			I			S
Signaling rate, each lane		25.78125± 100 ppm		0 ppm	Gb/s	
Lane Wavelength Range	Lane 0	1294.5	/	1296.5	nm	
		3		9		
	Lane 1	1299.0 2	/	1301.0 9	nm	
	Lane 2	1303.5	/	1305.6	nm	
	Lanc 2	4	,	3		
	Lane 3	1308.0	1	1310.1	nm	
		9		9		
Average Optical Power per lane		-4.3		4.5	dBm	
Total Average Launch Power				10.5	dBm	
Optical Modulation Amplitude (OMA), each lane		-1.3		4.5	dBm	
Launch Power in OMA minus TDP, each lane		-2.3			dBm	
Transmitter and Dispersion Penalty (TDP) each lane				2.2	dB	
Average Launch Power per Lane @ TX Off State				-30	dBm	
Extinction Ratio		4			dB	
Relative Intensity Noise (OMA)				-130	dB/Hz	
Side-Mode Suppression Ration (SMSR)		30			dB	
Optical Return Loss Tolerance				20	dB	
Transmitter Reflectance				-12	dB	
Transmitter Eye Mask Definition {X1, X2, X3, Y1, Y2, Y3}	{0	.25, 0.4, 0.	45, 0.25, 0.	.28, 0.4}		1
Transmitter Output Power Monitor Accuracy		-3		3	dB	
Receiver Parameter	Lane	Min	Typica	Max	Unit	Note
			1			s
Signaling rate, each lane		25.	78125± 100	0 ppm	Gb/s	
Lane Wavelength Range	Lane 0	1294.5	/	1296.5	nm	
		3		9		
	Lane 1	1299.0	/	1301.0	nm	
		2		9		
	Lane 2	1303.5	/	1305.6	nm	
	Lane 3	1308.0	/	3 1310.1	nm	
		9	'	9	''''	
Damage Threshold		5.5			dBm	
Average Receive Power, each lane		-10.6		4.5	dBm	
Receive Power, each lane (OMA)				4.5	dBm	
Receiver Reflectance				-26.0	dB	

Receiver Sensitivity (OMA) per lane		-8.6	dBm	2
Stressed receiver sensitivity(OMA),each lane		-6.8	dBm	3
Receive Power Monitor Accuracy	-3.0	3.0	dB	

Notes:

- 1. Hit ratio 5x10⁻⁵
- 2.Measured with a test pattern of PRBS 2³¹-1 at Pre-fec BER 1x10⁻¹²
- 3. Measured with vertical eye closure penalty of 1.8 dB max, J2 of 0.30 UI, and J9 of 0.47 UI.

OTU4 4I1-9D1F Operation

Transmitter Parameter	Lane	Min	Typical	Max	Unit	Notes
Signaling rate, each lane		27.	9525± 20 pp	m	Gb/s	
Lane Wavelength Range	Lane 0	1294.53	/	1296.59	nm	
	Lane 1	1299.02	/	1301.09	nm	
	Lane 2	1303.54	1	1305.63	nm	
	Lane 3	1308.09	1	1310.19	nm	
Average launch Power per channel		-0.6		4	dBm	
Total Average Launch Power				10	dBm	
Channel power difference				5	dB	
Extinction Ratio		4		7	dB	
Optical Return Loss				20	dB	
Transmitter Output Power Monitoring Accuracy		-3		3	dB	
Transmitter Eye Mask Definition {X1, X2, X3, Y1, Y2, Y3}	2, {0.25, 0.4, 0.45, 0.25, 0.28, 0.4}					1
Receiver Parameter	Lane	Min	Typical	Max	Unit	Notes
					S	
Signaling rate, each lane			9525± 20 pp		Gb/s	
Lane Wavelength Range	Lane 0	1294.53	/	1296.59	nm	
	Lane 1	1299.02	/	1301.09	nm	
	Lane 2	1303.54 1308.09	/	1305.63 1310.19	nm	
	Lane 3		/		nm	
Average Input Power per Channel		-6.9		4.0	dBm	
Total Average Input Power				10.0	dBm	
Optical Path penalty				1.5	dB	
Channel Power Difference				5.5	dB	
Receiver Reflectance				-26.0	dB	
Equivalent Sensitivity per Channel				-8.4	dBm	2
Receive Power Monitor Accuracy		-3.0		3.0	dB	

Notes:

- 1. Hit ratio 5x10⁻⁵
- 2.2.Measured with a test pattern of PRBS 231-1 at Pre-fec BER 1x10-6

QSFP28 Connector and Pinout Description

The electrical interface to the transceiver is a 38 pins edge connector. The 38 pins provide high speed data, low speed monitoring and control signals, I2C communication, power and ground connectivity. The top and bottom views of the connector are provided below, as well as a table outlining the contact numbering, symbol and full description.

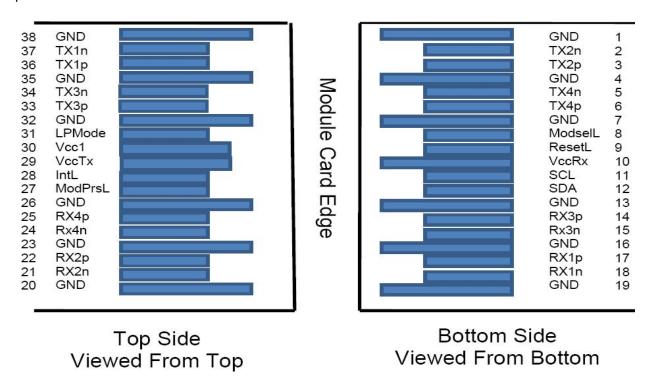


Figure 1. QSFP28-compliant 38-pin connector

QSFP Transceiver Pinout

Pin No.	Logic	Symbol	Description	Plug Sequence
1		GND	Ground	1
2	CML-I	TX2n	Transmitted Inverted Data Input	3
3	CML-I	TX2p	Transmitted Non-Inverted Data Input	3
4		GND	Ground	1
5	CML-I	TX4n	Transmitted Inverted Data Input	3
6	CML-I	TX4p	Transmitted Non-Inverted Data Input	3

7			1		
9 LVTTL-I ResetL. Module Reset 3 10 Vcc Rx +3.3 VDC Receiver Power Supply 2 11 LVCMOS-I/O SCL Serial Clock for I2C Interface 3 12 LVCMOS-I/O SDA Serial Data for I2C Interface 3 13 GND Ground 1 14 CML-O RX3p Receiver Non-Inverted Data Output 3 15 CML-O RX3n Receiver Inverted Data Output 3 16 GND Ground 1 17 CML-O RX1p Receiver Non-Inverted Data Output 3 18 CML-O RX1n Receiver Inverted Data Output 3 19 GND Ground 1 20 GND Ground 1 21 CML-O RX2p Receiver Inverted Data Output 3 22 CML-O RX4p Receiver Inverted Data Output 3 25 CML-O RX4p Receiver Non-Inverted Data Output 3	7		GND	Ground	1
10	8	LVTTL-I	ModSeil	Module Select	3
11 LVCMOS-I/O SCL Serial Clock for I2C Interface 3 12 LVCMOS-I/O SDA Serial Data for I2C Interface 3 13 GND Ground 1 14 CML-O RX3p Receiver Non-Inverted Data Output 3 15 CML-O RX3n Receiver Inverted Data Output 3 16 GND Ground 1 17 CML-O RX1p Receiver Non-Inverted Data Output 3 18 CML-O RX1n Receiver Inverted Data Output 3 19 GND Ground 1 20 GND Ground 1 21 CML-O RX2n Receiver Inverted Data Output 3 22 CML-O RX2p Receiver Non-Inverted Data Output 3 23 GND Ground 1 24 CML-O RX4p Receiver Inverted Data Output 3 25 CML-O RX4p Receiver Non-Inverted Data Output 3	9	LVTTL-I	ResetL	Module Reset	3
12 LVCMOS-I/O SDA Serial Data for I2C Interface 3 13 GND Ground 1 14 CML-O RX3p Receiver Non-Inverted Data Output 3 15 CML-O RX3n Receiver Inverted Data Output 3 16 GND Ground 1 17 CML-O RX1p Receiver Non-Inverted Data Output 3 18 CML-O RX1n Receiver Inverted Data Output 3 19 GND Ground 1 20 GND Ground 1 21 CML-O RX2n Receiver Inverted Data Output 3 22 CML-O RX4n Receiver Inverted Data Output 3 23 GND Ground 1 24 CML-O RX4n Receiver Inverted Data Output 3 25 CML-O RX4p Receiver Inverted Data Output 3 26 GND Ground 1 27 LVTL-O <td< td=""><td>10</td><td></td><td>Vcc Rx</td><td>+3.3 VDC Receiver Power Supply</td><td>2</td></td<>	10		Vcc Rx	+3.3 VDC Receiver Power Supply	2
13	11	LVCMOS-I/O	SCL	Serial Clock for I2C Interface	3
14 CML-O RX3p Receiver Non-Inverted Data Output 3 15 CML-O RX3n Receiver Inverted Data Output 3 16 GND Ground 1 17 CML-O RX1p Receiver Non-Inverted Data Output 3 18 CML-O RX1n Receiver Inverted Data Output 3 19 GND Ground 1 20 GND Ground 1 21 CML-O RX2n Receiver Inverted Data Output 3 22 CML-O RX2p Receiver Non-Inverted Data Output 3 23 GND Ground 1 24 CML-O RX4n Receiver Inverted Data Output 3 25 CML-O RX4p Receiver Inverted Data Output 3 26 GND Ground 1 27 LVTTL-O ModPrsL Module Present 3 28 LVTTL-O IntL Interrupt 3 29 Vcc	12	LVCMOS-I/O	SDA	Serial Data for I2C Interface	3
15 CML-O RX3n Receiver Inverted Data Output 3 16 GND Ground 1 17 CML-O RX1p Receiver Non-Inverted Data Output 3 18 CML-O RX1n Receiver Inverted Data Output 3 19 GND Ground 1 20 GND Ground 1 21 CML-O RX2n Receiver Inverted Data Output 3 22 CML-O RX2p Receiver Non-Inverted Data Output 3 23 GND Ground 1 24 CML-O RX4n Receiver Inverted Data Output 3 25 CML-O RX4p Receiver Inverted Data Output 3 26 GND Ground 1 27 LVTTL-O ModPlrsL Module Present 3 28 LVTTL-O ModPlrsL Module Present 3 29 Vcc Tx +3.3 VDC Power Supply 2 30 Vcc1 +3.3	13		GND	Ground	1
15 CML-O RX3n Receiver Inverted Data Output 3 16 GND Ground 1 17 CML-O RX1p Receiver Non-Inverted Data Output 3 18 CML-O RX1n Receiver Inverted Data Output 3 19 GND Ground 1 20 GND Ground 1 21 CML-O RX2n Receiver Inverted Data Output 3 22 CML-O RX2p Receiver Non-Inverted Data Output 3 23 GND Ground 1 24 CML-O RX4n Receiver Inverted Data Output 3 25 CML-O RX4p Receiver Inverted Data Output 3 26 GND Ground 1 27 LVTTL-O ModPlrsL Module Present 3 28 LVTTL-O ModPlrsL Module Present 3 29 Vcc Tx +3.3 VDC Power Supply 2 30 Vcc1 +3.3					
16 GND Ground 1 17 CML-O RX1p Receiver Non-Inverted Data Output 3 18 CML-O RX1n Receiver Inverted Data Output 3 19 GND Ground 1 20 GND Ground 1 21 CML-O RX2n Receiver Inverted Data Output 3 22 CML-O RX2p Receiver Inverted Data Output 3 23 GND Ground 1 24 CML-O RX4n Receiver Inverted Data Output 3 25 CML-O RX4p Receiver Inverted Data Output 3 26 GND Ground 1 27 LVTTL-O ModPrsL Module Present 3 28 LVTTL-O IntL Interrupt 3 29 Vcc Tx +3.3 VDC Transmitter Power Supply 2 30 Vcc1 +3.3 VDC Power Supply 2 31 LVTTL-I LPMode Low Power M	14	CML-O	RX3p	Receiver Non-Inverted Data Output	3
17 CML-O RX1p Receiver Non-Inverted Data Output 3 18 CML-O RX1n Receiver Inverted Data Output 3 19 GND Ground 1 20 GND Ground 1 21 CML-O RX2n Receiver Inverted Data Output 3 22 CML-O RX2p Receiver Non-Inverted Data Output 3 23 GND Ground 1 24 CML-O RX4n Receiver Inverted Data Output 3 25 CML-O RX4p Receiver Non-Inverted Data Output 3 26 GND Ground 1 27 LVTTL-O ModPrsL Module Present 3 28 LVTTL-O Intl. Interrupt 3 29 Vcc Tx +3.3 VDC Transmitter Power Supply 2 30 Vcc1 +3.3 VDC Power Supply 2 31 LVTTL-I LPMode Low Power Mode 3 32 GND	15	CML-O	RX3n	Receiver Inverted Data Output	3
18 CML-O RX1n Receiver Inverted Data Output 3 19 GND Ground 1 20 GND Ground 1 21 CML-O RX2n Receiver Inverted Data Output 3 22 CML-O RX2p Receiver Non-Inverted Data Output 3 23 GND Ground 1 24 CML-O RX4n Receiver Inverted Data Output 3 25 CML-O RX4p Receiver Non-Inverted Data Output 3 26 GND Ground 1 27 LVTTL-O ModPrsL Module Present 3 28 LVTTL-O IntL Interrupt 3 29 Vcc Tx +3.3 VDC Transmitter Power Supply 2 30 Vcc1 +3.3 VDC Power Supply 2 31 LVTTL-I LPMode Low Power Mode 3 32 GND Ground 1 33 CML-I TX3p Transmitted Inverted D	16		GND	Ground	1
19 GND Ground 1 20 GND Ground 1 21 CML-O RX2n Receiver Inverted Data Output 3 22 CML-O RX2p Receiver Non-Inverted Data Output 3 23 GND Ground 1 24 CML-O RX4n Receiver Inverted Data Output 3 25 CML-O RX4p Receiver Non-Inverted Data Output 3 26 GND Ground 1 27 LVTTL-O ModPrsL Module Present 3 28 LVTTL-O IntL Interrupt 3 29 Vcc Tx +3.3 VDC Transmitter Power Supply 2 30 Vcc1 +3.3 VDC Power Supply 2 31 LVTTL-I LPMode Low Power Mode 3 32 GND Ground 1 33 CML-I TX3p Transmitted Non-Inverted Data Input 3 34 CML-I TX1p Transmitted Non-	17	CML-O	RX1p	Receiver Non-Inverted Data Output	3
20 GND Ground 1 21 CML-O RX2n Receiver Inverted Data Output 3 22 CML-O RX2p Receiver Non-Inverted Data Output 3 23 GND Ground 1 24 CML-O RX4n Receiver Inverted Data Output 3 25 CML-O RX4p Receiver Non-Inverted Data Output 3 26 GND Ground 1 27 LVTTL-O ModPrsL Module Present 3 28 LVTTL-O IntL Interrupt 3 29 Vcc Tx +3.3 VDC Transmitter Power Supply 2 30 Vcc1 +3.3 VDC Power Supply 2 31 LVTTL-I LPMode Low Power Mode 3 32 GND Ground 1 33 CML-I TX3p Transmitted Non-Inverted Data Input 3 34 CML-I TX1p Transmitted Non-Inverted Data Input 3 36 CML-I <td>18</td> <td>CML-O</td> <td>RX1n</td> <td>Receiver Inverted Data Output</td> <td>3</td>	18	CML-O	RX1n	Receiver Inverted Data Output	3
21 CML-O RX2n Receiver Inverted Data Output 3 22 CML-O RX2p Receiver Non-Inverted Data Output 3 23 GND Ground 1 24 CML-O RX4n Receiver Inverted Data Output 3 25 CML-O RX4p Receiver Non-Inverted Data Output 3 26 GND Ground 1 27 LVTTL-O ModPrsL Module Present 3 28 LVTTL-O IntL Interrupt 3 29 Vcc Tx +3.3 VDC Transmitter Power Supply 2 30 Vcc1 +3.3 VDC Power Supply 2 31 LVTTL-I LPMode Low Power Mode 3 32 GND Ground 1 33 CML-I TX3p Transmitted Non-Inverted Data Input 3 34 CML-I TX1p Transmitted Non-Inverted Data Input 3 36 CML-I TX1p Transmitted Inverted Data Input 3	19		GND	Ground	1
22 CML-O RX2p Receiver Non-Inverted Data Output 3 23 GND Ground 1 24 CML-O RX4n Receiver Inverted Data Output 3 25 CML-O RX4p Receiver Non-Inverted Data Output 3 26 GND Ground 1 27 LVTTL-O ModPrsL Module Present 3 28 LVTTL-O IntL Interrupt 3 29 Vcc Tx +3.3 VDC Transmitter Power Supply 2 30 Vcc1 +3.3 VDC Power Supply 2 31 LVTTL-I LPMode Low Power Mode 3 32 GND Ground 1 33 CML-I TX3p Transmitted Non-Inverted Data Input 3 34 CML-I TX3n Transmitted Non-Inverted Data Input 3 35 GND Ground 1 36 CML-I TX1p Transmitted Non-Inverted Data Input 3 37 CM	20		GND	Ground	1
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24 CML-O RX4n Receiver Inverted Data Output 3 25 CML-O RX4p Receiver Non-Inverted Data Output 3 26 GND Ground 1 27 LVTTL-O ModPrsL Module Present 3 28 LVTTL-O IntL Interrupt 3 29 Vcc Tx +3.3 VDC Transmitter Power Supply 2 30 Vcc1 +3.3 VDC Power Supply 2 31 LVTTL-I LPMode Low Power Mode 3 32 GND Ground 1 33 CML-I TX3p Transmitted Non-Inverted Data Input 3 34 CML-I TX3n Transmitted Inverted Data Input 3 35 GND Ground 1 36 CML-I TX1p Transmitted Non-Inverted Data Input 3 37 CML-I TX1n Transmitted Inverted Data Input 3	22	CML-O	RX2p	Receiver Non-Inverted Data Output	3
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27 LVTTL-O ModPrsL Module Present 3 28 LVTTL-O IntL Interrupt 3 29 Vcc Tx +3.3 VDC Transmitter Power Supply 2 30 Vcc1 +3.3 VDC Power Supply 2 31 LVTTL-I LPMode Low Power Mode 3 32 GND Ground 1 33 CML-I TX3p Transmitted Non-Inverted Data Input 3 34 CML-I TX3n Transmitted Inverted Data Input 3 35 GND Ground 1 36 CML-I TX1p Transmitted Non-Inverted Data Input 3 37 CML-I TX1n Transmitted Inverted Data Input 3	25	CML-O	RX4p	Receiver Non-Inverted Data Output	3
28 LVTTL-O IntL Interrupt 3 29 Vcc Tx +3.3 VDC Transmitter Power Supply 2 30 Vcc1 +3.3 VDC Power Supply 2 31 LVTTL-I LPMode Low Power Mode 3 32 GND Ground 1 33 CML-I TX3p Transmitted Non-Inverted Data Input 3 34 CML-I TX3n Transmitted Inverted Data Input 3 35 GND Ground 1 36 CML-I TX1p Transmitted Non-Inverted Data Input 3 37 CML-I TX1n Transmitted Inverted Data Input 3	26		GND	Ground	1
29 Vcc Tx +3.3 VDC Transmitter Power Supply 2 30 Vcc1 +3.3 VDC Power Supply 2 31 LVTTL-I LPMode Low Power Mode 3 32 GND Ground 1 33 CML-I TX3p Transmitted Non-Inverted Data Input 3 34 CML-I TX3n Transmitted Inverted Data Input 3 35 GND Ground 1 36 CML-I TX1p Transmitted Non-Inverted Data Input 3 37 CML-I TX1n Transmitted Inverted Data Input 3	27	LVTTL-O	ModPrsL	Module Present	3
30 Vcc1 +3.3 VDC Power Supply 2 31 LVTTL-I LPMode Low Power Mode 3 32 GND Ground 1 33 CML-I TX3p Transmitted Non-Inverted Data Input 3 34 CML-I TX3n Transmitted Inverted Data Input 3 35 GND Ground 1 36 CML-I TX1p Transmitted Non-Inverted Data Input 3 37 CML-I TX1n Transmitted Inverted Data Input 3	28	LVTTL-O	IntL	Interrupt	3
31 LVTTL-I LPMode Low Power Mode 3 32 GND Ground 1 33 CML-I TX3p Transmitted Non-Inverted Data Input 3 34 CML-I TX3n Transmitted Inverted Data Input 3 35 GND Ground 1 36 CML-I TX1p Transmitted Non-Inverted Data Input 3 37 CML-I TX1n Transmitted Inverted Data Input 3	29		Vcc Tx	+3.3 VDC Transmitter Power Supply	2
32 GND Ground 1 33 CML-I TX3p Transmitted Non-Inverted Data Input 3 34 CML-I TX3n Transmitted Inverted Data Input 3 35 GND Ground 1 36 CML-I TX1p Transmitted Non-Inverted Data Input 3 37 CML-I TX1n Transmitted Inverted Data Input 3	30		Vcc1	+3.3 VDC Power Supply	2
33 CML-I TX3p Transmitted Non-Inverted Data Input 3 34 CML-I TX3n Transmitted Inverted Data Input 3 35 GND Ground 1 36 CML-I TX1p Transmitted Non-Inverted Data Input 3 37 CML-I TX1n Transmitted Inverted Data Input 3	31	LVTTL-I	LPMode	Low Power Mode	3
34 CML-I TX3n Transmitted Inverted Data Input 3 35 GND Ground 1 36 CML-I TX1p Transmitted Non-Inverted Data Input 3 37 CML-I TX1n Transmitted Inverted Data Input 3	32		GND	Ground	1
35 GND Ground 1 36 CML-I TX1p Transmitted Non-Inverted Data Input 3 37 CML-I TX1n Transmitted Inverted Data Input 3	33	CML-I	TX3p	Transmitted Non-Inverted Data Input	3
36 CML-I TX1p Transmitted Non-Inverted Data Input 3 37 CML-I TX1n Transmitted Inverted Data Input 3	34	CML-I	TX3n	Transmitted Inverted Data Input	3
37 CML-I TX1n Transmitted Inverted Data Input 3	35		GND	Ground	1
37 CML-I TX1n Transmitted Inverted Data Input 3					
'			· ·	•	I .
38		CML-I		•	
	38		GND	Ground	1

High Speed Electrical Characteristics

Transmitter Parameter	Min	Typical	Max	Unit
Signaling rate per lane (range)	25.78	3125 ± 100 ppm		GBd
AC common-mode output voltage (RMS)			17.5	m
				V
Differential output voltage			900	m V
Eye width	0.57			UI
Eye height, differential	228			m V
Vertical eye closure			5.5	d
				В
Differential output return loss	Equation (83E–2)			d B
Common to differential mode conversion return loss	Equation			d
	(83E-3)			В
Differential termination mismatch			10	%
Transition time (20% to 80%)	12			р
				s
DC common mode voltage	-350		2850	m V
Receiver Parameter	Min	Typical	Max	Unit
Signaling rate per lane (range)	25.78	3125 ± 100 ppm		GBd
AC common-mode output voltage (RMS)			17.5	m V
Differential output voltage			900	m V
Eye width	0.57			UI
Eye height, differential	228			m V
Vertical eye closure			5.5	d
				В
Differential output return loss	Equation			d B
	(83E-2)			
Common to differential mode conversion return loss	Equation			d
	(83E-3)			В
Differential termination mismatch			10	%
Transition time (20% to 80%)	12			р
				S

Functional Block Diagram

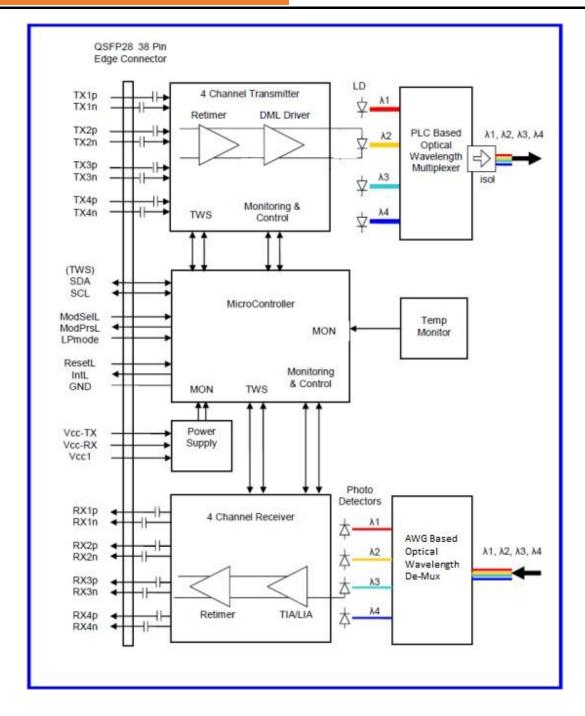


Figure 2. Functional Block Diagram

Mechanical Specifications

Pull Tab Pantone: Blue

Pantone: 300U

Unit: mm

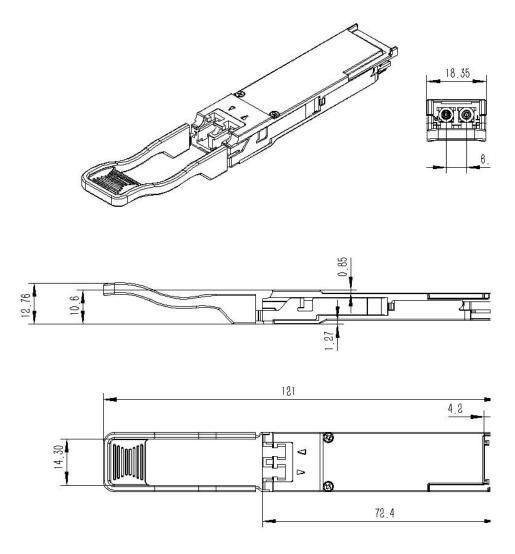


Figure 3. Mechanical Dimensions

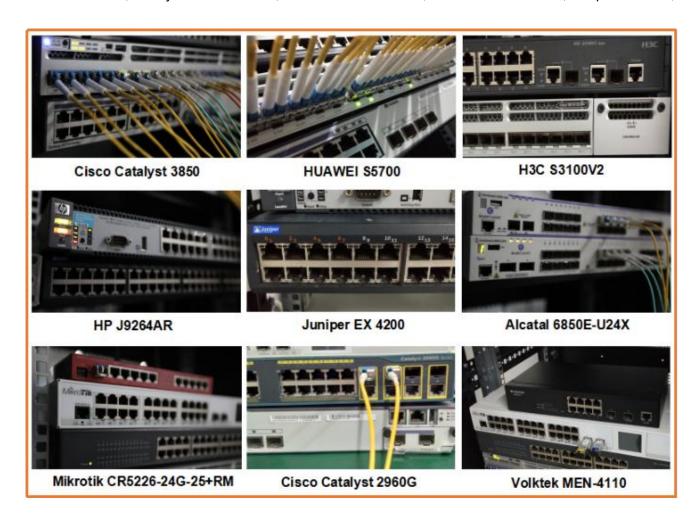
Ordering Information

Part Number	Product Description
EQ231M10X-3LCD10	100G and 112G Dual Rate QSFP28 LR4 10KMOptical Transceiver

Compatibility Test

In order to ensure the product compatibility, our products will be tested on the switch before shipment. Our modules can compatible with many mainstream brand switches, such as Cisco, Juniper, Extreme, Brocade, IBM, H3C, HP, Huawei, D-Link, Mikrotik, ZTE, TP-Link...

Our test equipment: VOLKTEK MEN-4110, HP 2530-8G, CRS226-24G-25+RM, Catalyst 2960G Series, Catalyst 3850 XS 10G SFP+, Catalyst 3750-E Series, HUAWEI S5700Series, H3C S3100V2 Series, Juniper-EX4200, etc.



Product Production Process

Quality Assurance

Continuous introduction of new equipment, produced by strict standards, strict quality inspection, to guarantee the high quality standard of each product.



Packaging

ETU-Link provides two kinds of packaging, 10pcs/Tray and individual package.



Company: ETU-Link Technology Co., LTD

Address: Right side of 3rd floor, No. 102 building, Longguan expressway, Dalang street, Longhua District,

Shenzhen city, GuangDongProvince,China

Tel: +86-755 2328 4603

Addresses and phone number also have been listed at www.etulinktechnology.com.

Please e-mail us at sales@etulinktechnology.com or call us for assistance.