ESX-LBxx

10Gb/s SFP+ Electrical Passive Loopback

PRODUCT FEATURES

- SFP+ MSA Compliant
- Hot-pluggable MSA foot print
- Custom Memory Maps Capability
- Case Temperature range from -20° to 85°C
- Compliant with SONET, SDH, GBE, FC
- Power Consumption Different Option
- Internal Attenuation Different Option

APPLICATIONS

- Board and System Level Testing
- Test and Measurement
- Switch and Router Chamber Testing ---HASS and HALT
- 100Mb/s to 10.5Gbps

DESCRIPTIONS

10G SFP+ Loopback modules provide an effective way of testing the SFP+ port in the host system by looping back the electrical signal (optics are excluded). The units provide basic serial ID information that attempts to mimic a shortwave Gigabit Ethernet, 1.25G,2. 125G FC SFP transceiver, 4.25G FC, 8.5G FC and 10Gb/s Ethernet/FC for factory,environment, installation, simulation tests.

Ordering Information

Part Number	Internal Attenuation	Power Consumption	Product description
ESX-LB0	0dB	1W	SFP loopback 0dB
ESX-LB3.5	3.5 dB	1.5W	SFP loopback 3.5dB
ESX-LB5	5 dB	2.5W	SFP loopback 5dB

Notes: Maximum total power value is specified across the full temperature and voltage range and may vary according to different Options (0~2.5W).

Absolute Maximum Ratings

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Storage Temperature	Tstg	-40		85	ºC	
Supply Voltage	Vcc			6.00	V	Vcc-ground
Data DC Voltage	Voffset	-10		10	Vpk	V (Tx+, Tx-, Rx+, Rx-) to ground

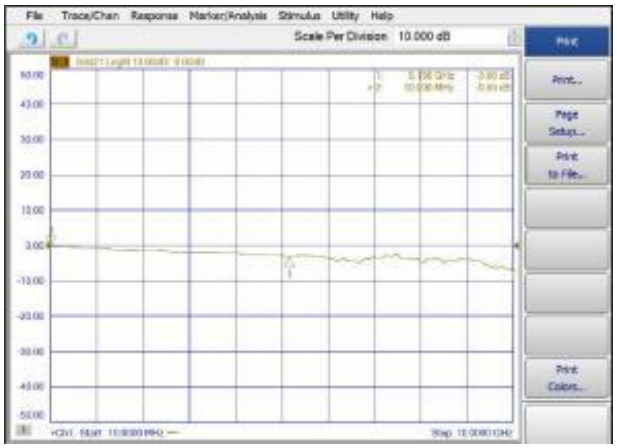
Recommended Operating Conditions

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Ambient Operating Temperature	Ta	-20		85	ºC	
Supply Voltage	Vcc	3.15	3.3	3.45	Vdc	
Baud Rate	BRate	0.1		10.5	Gpbs	

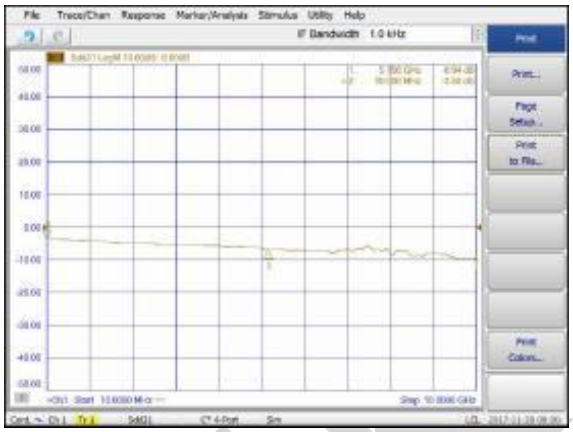
DATA PATH

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Impedance			100		ohms	Differential Impedance

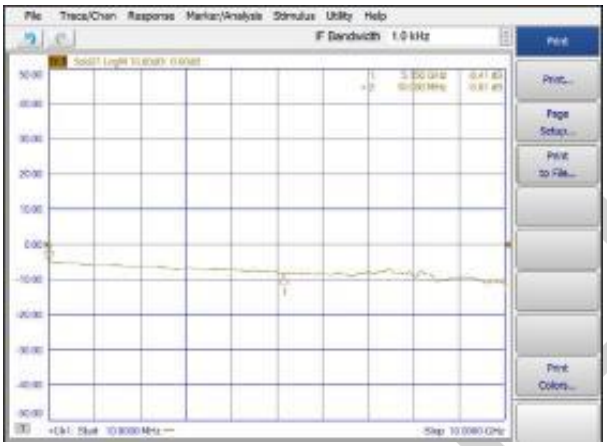
Durability Cycles			100		Times	



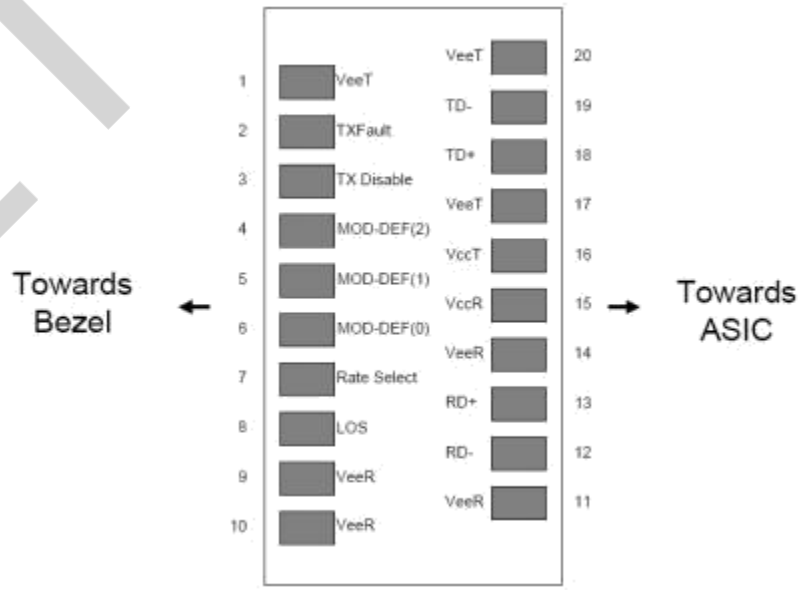
SDD12-0dB (Transmit Insertion Loss)



SDD21-3.5dB (Transmit Insertion Loss)



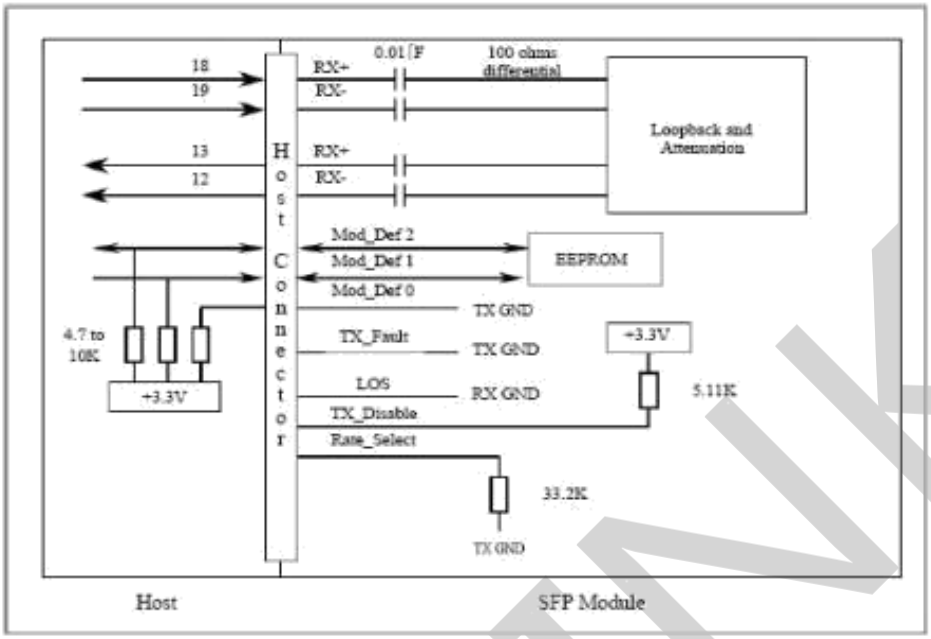
Pin Diagram



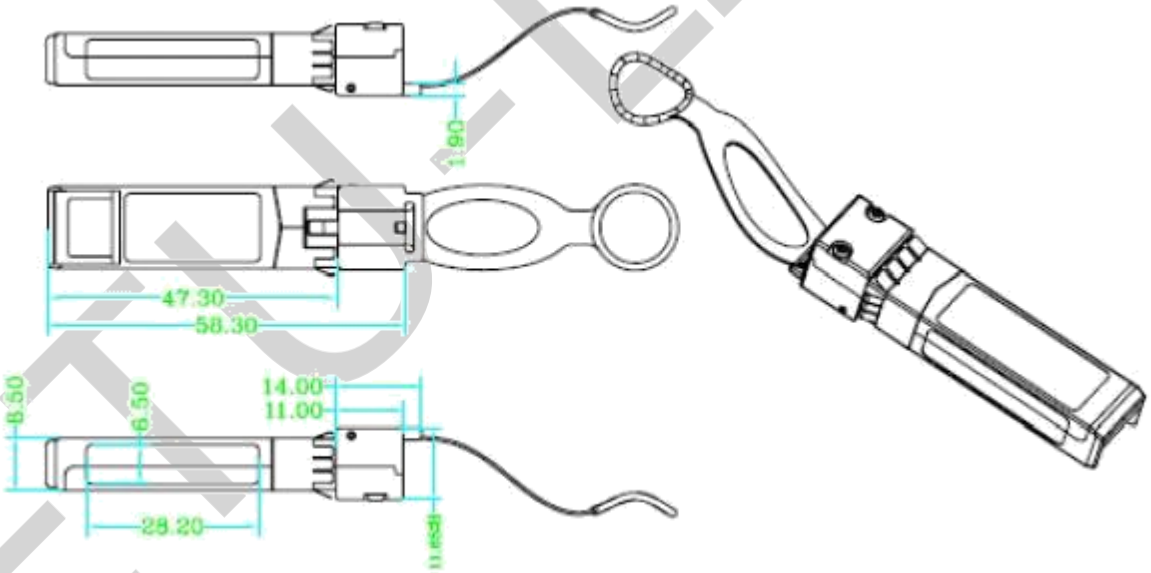
Pin Definitions

Pin	Logic	Description
1	TGND	Transmit ground
2	TX_FAULT	Internally tied to Transmit ground. TX_FAULT is not implemented.
3	TX_DISABLE	Internally pulled up to Vcc through a 5.11k ohm resistor. TX_DISABLE is not implemented.
4	MOD_DEF(2)	Signal SDA (Data) of the 2-wire serial ID interface
5	MOD_DEF(1)	Signal SCL (Clock) of the 2-wire serial ID interface
6	MOD_DEF(0)	This pin is internally tied to Transmit ground
7	RATE SELECT	Pin is internally pulled low through a 33.2k resistor. Rate Select is not implemented.
8	LOS	Internally tied to Receiver Ground. LOS is not implemented.
9	RGND	Receiver ground
10	RGND	Receiver ground
11	RGND	Receiver ground
12	RD-	Differential receiver outputs. User to terminate to 100 ohms differential
13	RD+	Differential receiver outputs. User to terminate to 100 ohms differentia
14	RGND	Receiver ground
15	VCCR	Not used.
16	VCCT	EEPROM power
17	TGND	Transmit ground
18	TD+	Differential transmitter inputs. Internally terminated to 100 ohms differential.
19	TD-	Differential transmitter inputs. Internally terminated to 100 ohms differential.
20	TGND	Transmit ground

Recommended Interface Circuit



Mechanical Diagram



Revision History

Version No.	Date	Description
1.0	February 18, 2019	Preliminary datasheet
2.0	Aug 28, 2024	Format change

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