EQD400-DR4+

400G QSFP-DD DR4+ Optical Transceiver

PRODUCT FEATURES

- Compliant to QSFP-DD MSA
- Parallel 4 Optical Lanes
- IEEE 802.3bs 400GBASE-DR4 Specification compliant
- Maximum power consumption 9.5W
- Compliant with IEEE Std 802.3bs
- Compliant with 400G-DR4 optical specifications
- Compliant with CMIS4.0 Management interface specifications
- 8x53.125Gb/s electrical interface (400GAUI-8)
- Up to 2km transmission on single mode fiber (SMF) with FEC
- Single +3.3V power supply
- Case temperature range: 0 ~ +70℃
- RoHS complaint

APPLICATIONS

- 400G Ethernet
- Data Center Interconnect
- Infiniband Interconnect
- Enterprise Networking

ETU-LINK

DESCRIPTIONS

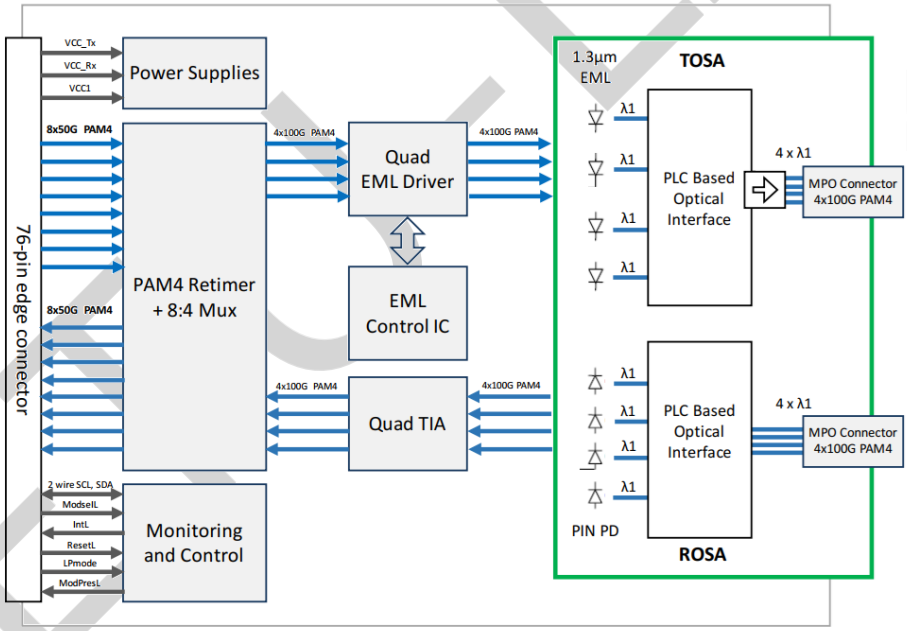
This product is a 400Gb/s QSFP-DD optical module designed for 2Km optical communication applications. The module converts 8 channels of 50Gb/s (PAM4) electrical input data to 4 channels of parallel optical signals, each capable of 100Gb/s operation for an aggregate data rate of 400Gb/s.

On the receiver side, the module converts 4 channels of parallel optical signals of 100Gb/s each channel for an aggregate data rate of 400Gb/s into 8 channels of 50Gb/s (PAM4) electrical output data.

An optical fiber cable with an MTP/MPO-12 connector can be plugged into the QSFP-DD DR4+ module receptacle. Host FEC is required to support up to 2Km fiber transmission.

This transceiver is based on proprietary ETU-LINK technology, using surface mounted opto-electronic devices with no free space elements. The unique design of the optical engine facilitates unparalleled compactness while maintaining Telcordia robustness.

Module Block Diagram



Ordering Information

Part No.	Description
EQD400-DR4+	400G QSFP-DD DR4+ Optical Transceiver

Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Units
Storage Temperature Range	TSTG	-40	+85	ºC
Supply Voltage	VCC	0	4	V
Relative Humidity	RH	10% to 90% non-condensing		

Recommended Operating Conditions

Parameter	Symbol	Min	Max	Unit
Case Temperature- Operating	TCASE	0	70	ºC
Supply Voltage	Vcc	3.14	3.46	V
Power Consumption	PDISS		12	W
Pre-FEC Bit Error Ratio			$2.4x10^{-4}$	
Post-FEC Bit Error Ratio			$1x10^{-12}$	
Link Distance		2	2000	M

High Speed Electrical Specification

Parameter	Min	Typical	Max	Unit	Notes
Receiver electrical output characteristics at TP4					
Signaling rate per lane		26.5625		GBd	
AC common-mode output voltage(RMS)		-	17.5	mV	
Differential peak-to-peak output voltage			900	mV	
Near-end SMW(Eye symmetry mask width)		0.265		UI	
Near-end Eye height, differential	70			mV	
Far-end ESMW(Eye symmetry mask width)		0.2		UI	
Far-end Eye height, differential	30			mV	
Far-end pre-cursor ISI ratio	-4.5		2.5	%	
Differential output return loss	9.5-0.37f			dB	0.01-8 GHz
	4.75-7.4log 10(f/14)			dB	8-19 GHzGHz
Common to differential mode conversion return loss	22-20(f/25.78)			dB	0.01-12.89 GHz
	15-6log 10(f/25.78)			dB	12.89-19GHz
Differential termination mismatch			10	%	
Transition time(min,20% to 80%)	9.5			ps	
DC common mode voltage	-350		2850	mV	

Transmitter electrical input characteristics at TP1					
Signaling rate per lane		26.5625		GBd	
Differential pk-pk input voltage tolerance	900			mV	
Differential input return loss	9.5-0.37f			dB	0.01-8 GHz
	4.75-7.4lg 10(f/14)			dB	8-19GHz
Differential to common mode input return loss	22-20(f/25.78)			dB	0.01-12.89GHz
	15-6log 10(f/25.78)			dB	12.89-19GHz
Differential termination mismatch			10	%	
Module stressed input test	Per Section 120E.3.4.1 IEEE802.3bs				
Single-ended voltage tolerance range	-0.4		3.3	V	
Common-mode voltage	-350		2850	mV	

Optical and Characteristics

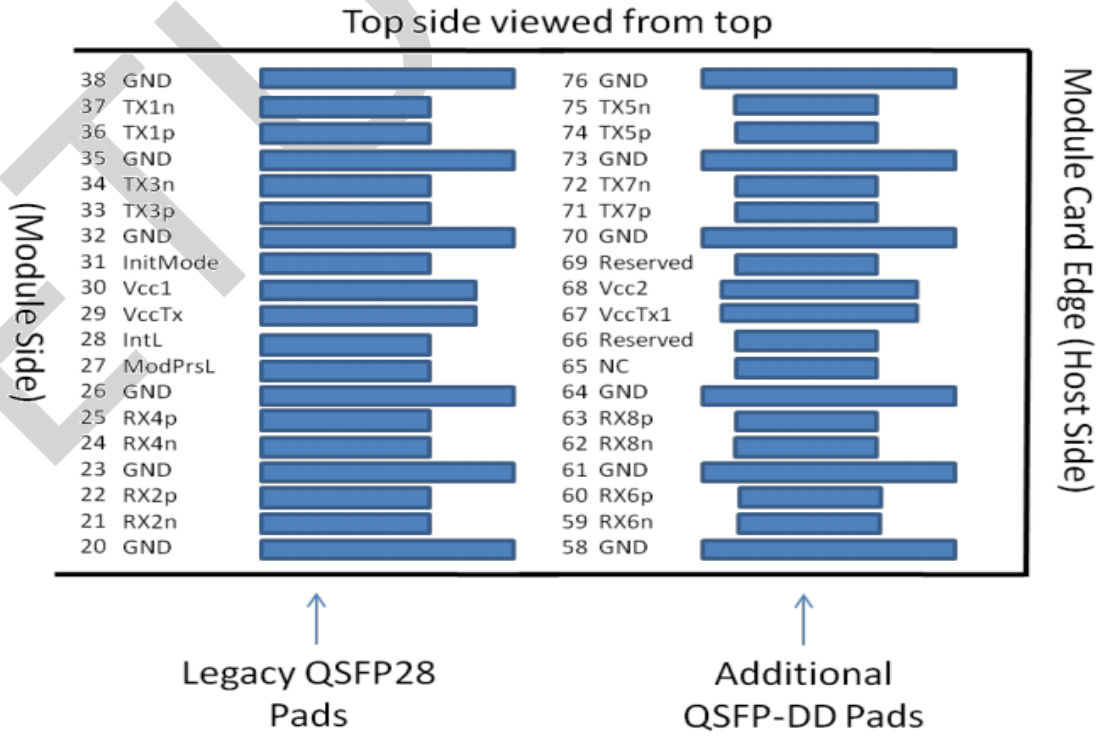
Parameter	Min	Typical	Max	Unit
Transmitter				
Lane Wavelength Range	1304.5	1310	1317.5	nm
Modulation Format		PAM4		
Average Optical Power per lane	-2.4		4	dBm
Outer Optical Modulation Amplitude (OMAouter), each lane	-0.2		4.2	dBm
Average Launch Power per Lane @ TX Off State			-15	dBm
Launch Power in OMAouter minus TDECQ, each Lane for ER ≥ 5dB for ER <5dB			 -1.6 -1.5	dBm
Transmitter and Dispersion Eye Closure for PAM4, each Lane			3.4	dB
Extinction Ratio	3.5			dB
Relative Intensity Noise (OMA)			-136	dB/Hz
Side-Mode Suppression Ration (SMSR)	30			dB
Optical Return Loss Tolerance			17.1	dB
Transmitter Reflectance			-26	dB
Lane Wavelength Range	1304.5		1317.5	nm
Modulation Format		PAM4		
Damage Threshold	5.0			dBm
Average Receive Power, each lane	-5.9		4.0	dBm
Receiver Power, each lane (OMA)			4.2	dBm

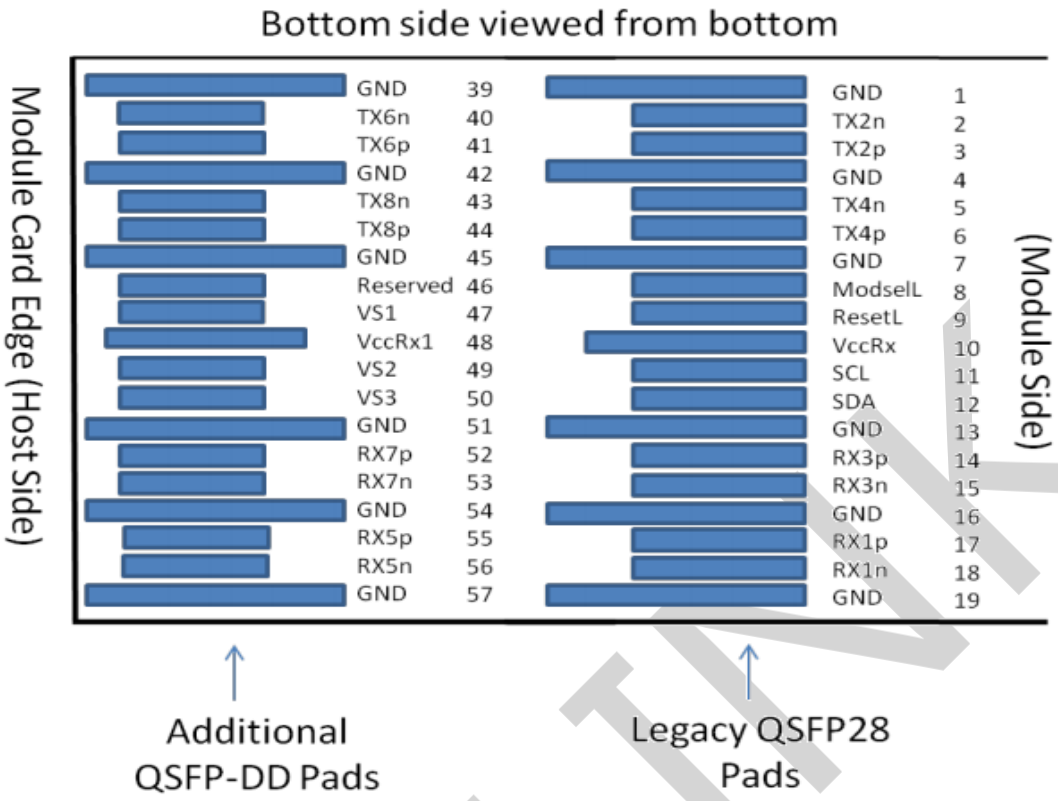
Receiver Reflectance			-26.0	dB
Receiver Sensitivity each lane (OMA outer)			-4.4	dBm
Stressed Receiver Sensitivity (OMA outer), each			-1.9	dBm
Stressed Conditions for Stress Receiver Sensitivity				
Stressed Eye Closure for PAM4 (SECQ),Lane under Test		3.4		dB
OMA outer of each Aggressor Lane		4.2		dBm
Rx_LOS_Assert Min/Max	-15.0			dBm
RX_LOS_De-Assert Min/Max			-8.9	dBm
RX_LOX_Hysteresis		1.5		dB

Digital Diagnostics

Parameters	Unit	Specification
Temperature Monitor absolute error	° C	±3
Supply Voltage Monitor absolute error	%	±5
I_bias Monitor absolute error	%	±10
Received Power (Rx) Monitor absolute error	dB	±3.0
Transmit Power (Tx) Monitor absolute error	dB	±3.0

Pin Diagram





Pin Definitions

Pin No.	Symbol	Description	Notes
1	GND	Ground	1
2	TX2n	Transmitted Inverted Data Input	
3	TX2p	Transmitted Non-Inverted Data Output	
4	GND	Ground	1
5	TX4n	Transmitted Inverted Data Input	
6	TX4p	Transmitted Non-Inverted Data Output	
7	GND	Ground	1
8	ModSEIL	Module Select	
9	ResetL	Module Reset	
10	Vcc Rx	+3.3 Power Supply Receiver	2
11	SCL	2-Wire serial Interface Clock	
12	SDA	2-Wire serial Interface Data	
13	GND	Ground	1
14	RX3p	Receiver Non-Inverted Data Output	
15	RX3n	Receiver Inverted Data Output	
16	GND	Ground	1

17	RX1p	Receiver Non-Inverted Data Output	
18	RX1n	Receiver Inverted Data Output	
19	GND	Ground	1
20	GND	Ground	1
21	RX2n	Receiver Inverted Data Output	
22	RX2p	Receiver Non-Inverted Data Output	
23	GND	Ground	1
24	RX4n	Receiver Inverted Data Output	
25	RX4p	Receiver Non-Inverted Data Output	
26	GND	Ground	1
27	ModPrsL	Module Present	
28	IntL	Interrupt	
29	VccTx	3.3V Power Supply Transmitter	2
30	Vcc1	3.3V Power Supply	2
31	Init Mode	Initialization mode	
32	GND	Ground	1
33	TX3p	Transmitted Non-Inverted Data Input	
34	TX3n	Transmitted Inverted Data Output	
35	GND	Ground	1
36	TX1p	Transmitted Non-Inverted Data Input	
37	TX1n	Transmitted Inverted Data Output	
38	GND	Ground	1
39	GND	Ground	1
40	TX6n	Transmitter Inverted Data Input	
41	TX6p	Transmitter Non-Inverted Data output	
42	GND	Ground	1
43	TX8n	Transmitter Inverted Data Input	
44	TX8p	Transmitter Non-Inverted Data output	
45	GND	Ground	1
46	Reserved	For Future Use	3
47	VS1	Module Vendor Specific 1	3
48	VccRx1	3.3V Power Supply	2
49	VS2	Module Vendor Specific 2	3
50	VS3	Module Vendor Specific 3	3
51	GND	Ground	1
52	RX7p	Receiver Non-Inverted Data Output	

53	RX7n	Receiver Inverted Data Output	
54	GND	Ground	1
55	RX5p	Receiver Non-Inverted Data Output	
56	RX5n	Receiver Inverted Data Output	
57	GND	Ground	1
58	GND	Ground	1
59	RX6n	Receiver Inverted Data Output	
60	RX6p	Receiver Non-Inverted Data Output	
61	GND	Ground	1
62	RX8n	Receiver Inverted Data Output	
63	RX8p	Receiver Non-Inverted Data Output	
64	GND	Ground	1
65	NC	No Connect	3
66	Reserved	For Future Use	3
67	VccTx1	3.3V Power Supply	2
68	Vcc2	3.3V Power Supply	2
69	Reserved	For Future Use	3
70	GND	Ground	1
71	Tx7p	Transmitter Non-Inverted Data output	
72	Tx7n	Transmitter Inverted Data output	
73	GND	Ground	1
74	Tx5p	Transmitter Non-Inverted Data input	
75	Tx5n	Transmitter Inverted Data output	
76	GND	Ground	1

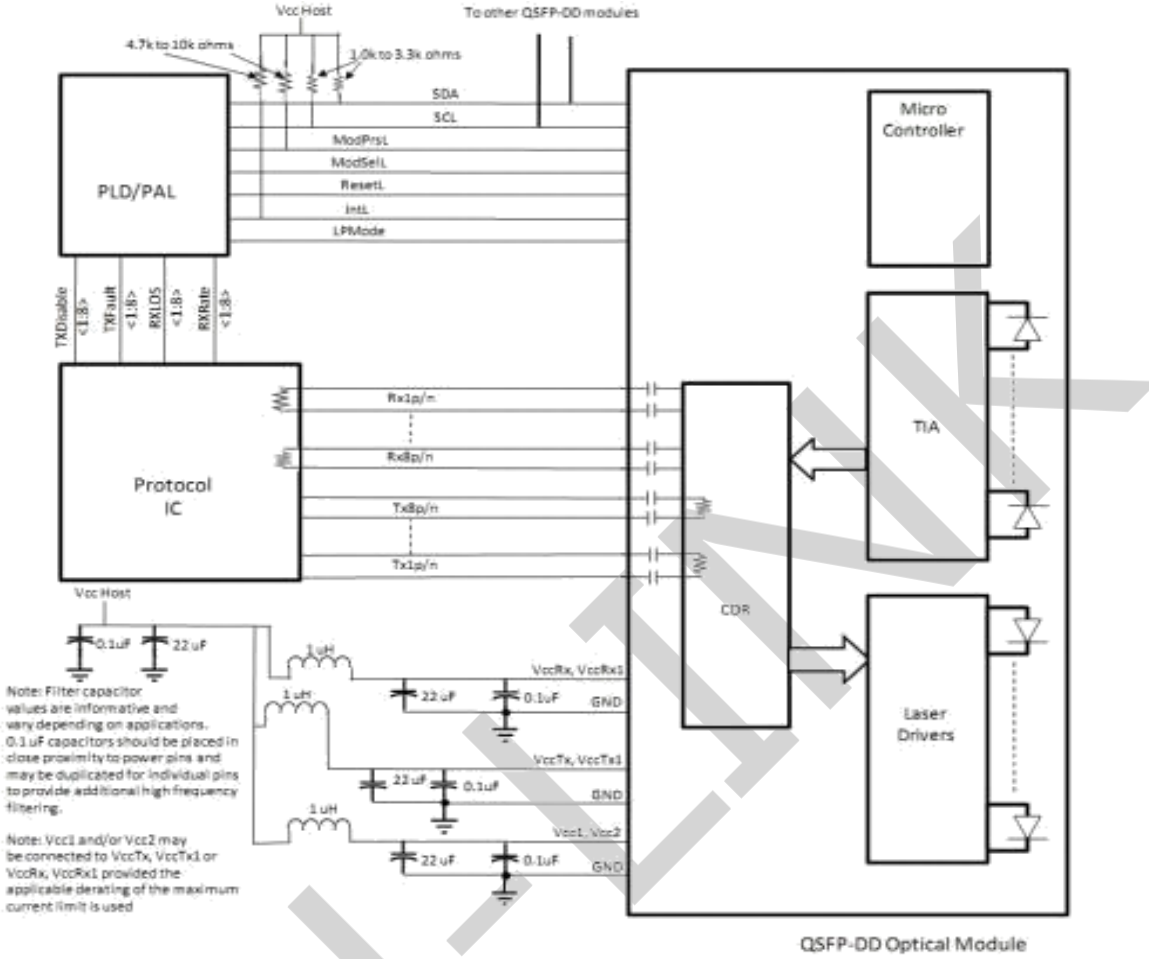
Note：

1．QSFP-DD uses common ground (GND)for all signals and supply (power). All are common within the QSFP-DD module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane.

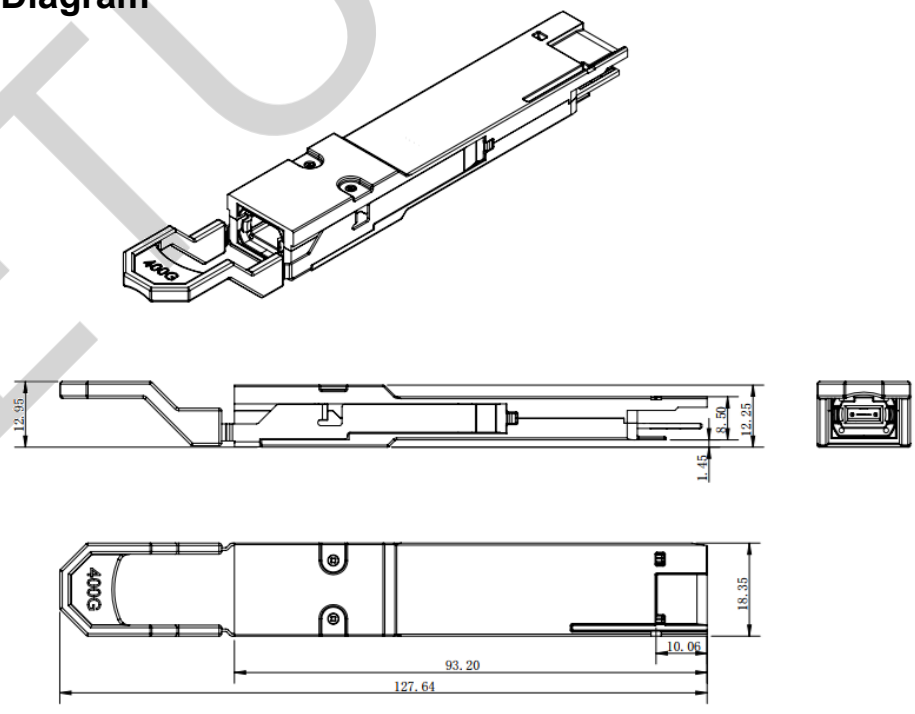
2．VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 shall be applied concurrently. Requirements defined for the host side of the Host Card Edge Connector are listed in Table 8. VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 may be internally connected within the module in any combination. For power classes 4 and above the module differential loading of input voltage pins must not result in exceeding pin current limits. The connector Vcc pins are each rated for a maximum current of 1000 mA.

3． All Vendor Specific, Reserved, No Connect and ePPS (if not used) pins may be terminated with 50 □ to ground on the host. Pad 65 (No Connect) shall be left unconnected within the module. Vendor specific and Reserved pads shall have an impedance to GND that is greater than 10 k□ and less than 100 pF.

Recommended Interface Circuit



Mechanical Diagram



Revision History

Version No.	Date	Description
1.0	February 18, 2022	Preliminary datasheet
2.0	July 13,2024	Format change

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