EAQD400-QPxx

400Gb/s QSFP-DD TO 2*200G QSFP56 Active Optical Cable

PRODUCT FEATURES

- 400Gb/s to 2x200Gb/s data rate
- 8x 50Gb/s PAM4 modulation
- Single 3.3V power supply
- Max 4.5W power dissipation each QSFP56 end
- Max 8W power dissipation QSFP-DD end
- Compliant to CMIS V4.0
- Operating case temp Commercial: 0°C to +70 °C
- Hot pluggable
- RoHS compliant

APPLICATIONS

- 400Gb/s systems
- Other optical links

Description

The 400G QSFP56-DD to 2x 200G QSFP56 Breakout AOC are designed for 2x 200 Gigabit Ethernet links over multimode fiber, which provides connectivity between system units with a 400GbE connector on one side and two separate 200GbE connectors on the other two sides.

Ordering Information

Part No.	Data Rate(optical)	Laser	Fiber Type	Distance	Temp	DDMI
EAQD400-QPxx	425	PAM4	MMF	0.5~50m	0□~+70□	YES

Note:

1. where "x" denotes cable length in meters. Examples are as follows:
2. x = 1 for 1m, xx=10 for 10m

Absolute Maximum Ratings

Parameter	Symbol	Min.	Typical	Max.	Unit	Notes
Supply Voltage	Vcc3	-0.5	-	+3.6	V	
Storage Temperature	Ts	-10	-	+70	°C	
Operating Humidity	RH	+5	-	+85	%	

Recommended Operating Conditions

Parameter	Symbol	Min.	Typical	Max.	Unit	Notes
Operating Case Temperature	TC	0	-	+70	°C	
Power Supply Voltage	Vcc	3.135	3.3	3.465	V	
Power dissipation (400G retiming on all lanes)	Pd400G	-	-	8	W	1
Power dissipation (200G retiming on all lanes)	Pd200G	-	-	4.5	W	1

Electrical Characteristics

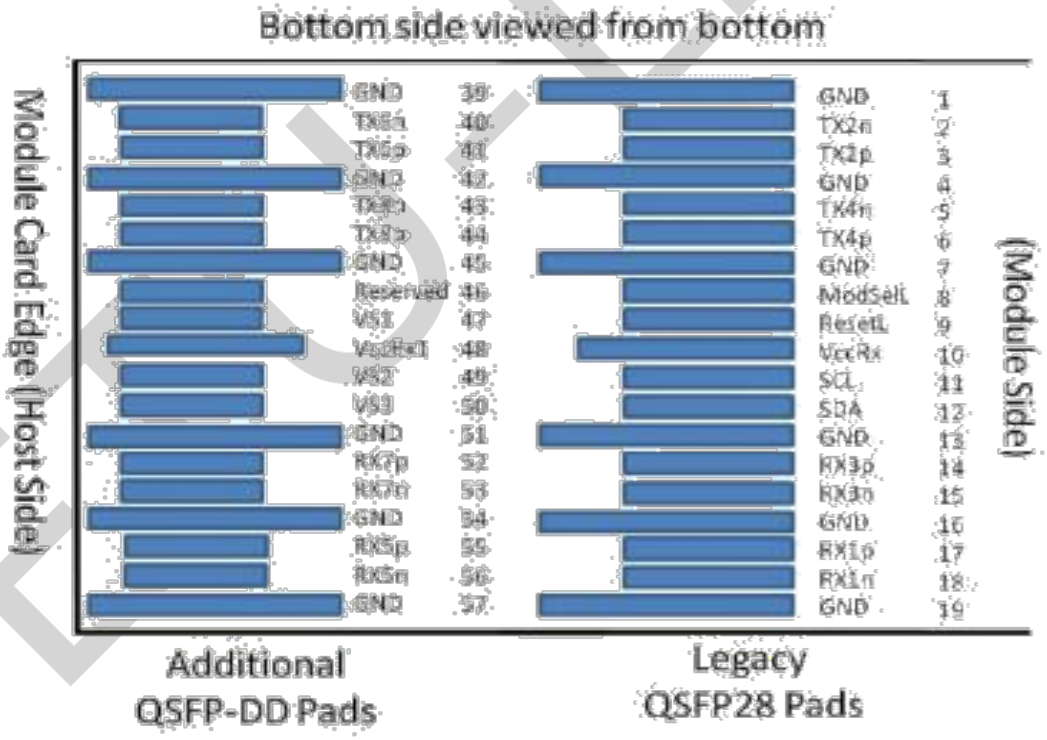
Parameter	Symbol	Unit	Min	Typ	Max	Notes
Transmitter						
Signaling rate (each lane)	SR	GBaud	26.5625 ± 100 ppm			
Differential data input voltage per lane	Vin,pp,diff	mV	-	-	900	
Differential termination mismatchal	-	%	-	-	10	

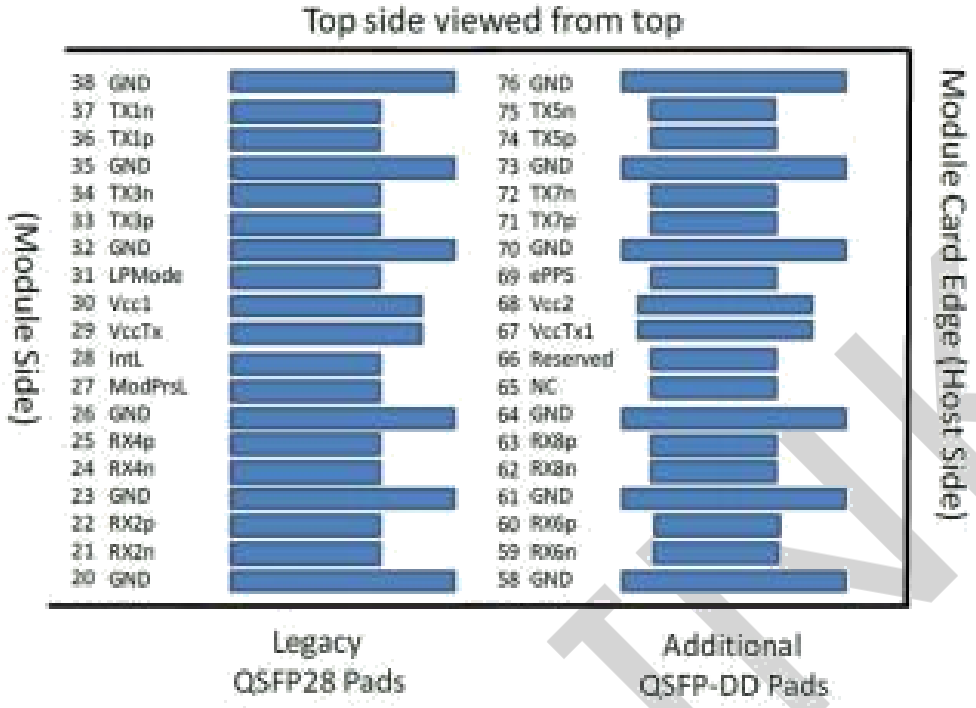
Single-ended voltage tolerance range	-	V	-0.4	-	3.3	
DC common mode voltage	-	mV	-350	-	2850	
Receiver						
Signaling rate (each lane)	SR	GBaud	26.5625 ± 100 ppm			
Differential output voltage	-	mV	-	-	900	
Differential termination mismatch	-	%	-	-	10	
Transition time (min, 20% to 80%)	-	ps	9.5	-	-	
DC common mode voltage	-	mV	-350	-	2850	
Error Bit Rate	BER	-	-	-	2.4E-4	Note1

Note: 1 PRBS31Q@26.5625Gbd PAM4

Pin Diagram

QSFP-DD end





Pin	Name	Logic	Description	Power Seq	Notes
1	Ground		GND	1B	1
2	Tx2n	CML-I	Transmitter Inverted Data Input	3B	
3	Tx2p	CML-I	Transmitter Non-Inverted Data Input	3B	
4	Ground		GND	1B	1
5	Tx4n	CML-I	Transmitter Inverted Data Input	3B	
6	Tx4p	CML-I	Transmitter Non-Inverted Data Input	3B	
7	Ground		GND	1B	1
8	ModSelL	LVTTL-I	Module Select	3B	
9	ResetL	LVTTL-I	Module Reset	3B	
10	VccRx		+3.3V Power Supply Receiver	2B	2
11	SCL	LVCMOS-I/O	2-wire serial interface clock	3B	
12	SDA	LVCMOS-I/O	2-wire serial interface data	3B	
13	Ground		GND	1B	1
14	Rx3p	CML-O	Receiver Non-Inverted Data Output	3B	
15	Rx3n	CML-O	Receiver Inverted Data Output	3B	

16	Ground		GND	1B	1
17	Rx1p	CML-O	Receiver Non-Inverted Data Output	3B	
18	Rx1n	CML-O	Receiver Inverted Data Output	3B	
19	Ground		GND	1B	1
20	Ground		GND	1B	1
21	Rx2n	CML-O	Receiver Inverted Data Output	3B	
22	Rx2p	CML-O	Receiver Non-Inverted Data Output	3B	
23	Ground		GND	1B	1
24	Rx4n	CML-O	Receiver Inverted Data Output	3B	
25	Rx4p	CML-O	Receiver Non-Inverted Data Output	3B	
26	Ground		GND	1B	1
27	ModPrsL	LVTTL-O	Module Present	3B	
28	IntL	LVTTL-O	Interrupt	3B	
29	VccTx		+3.3V Power supply transmitter	2B	2
30	Vcc1		+3.3V Power supply	2B	2
31	LPMode	LVTTL-I	Low Power mode	3B	
32	Ground		GND	1B	1
33	Tx3p	CML-I	Transmitter Non-Inverted Data Input	3B	
34	Tx3n	CML-I	Transmitter Inverted Data Input	3B	
35	Ground		GND	1B	1
36	Tx1p	CML-I	Transmitter Non-Inverted Data Input	3B	
37	Tx1n	CML-I	Transmitter Inverted Data Input	3B	
38	Ground		GND	1B	1
39	Ground		GND	1A	1
40	Tx6n	CML-I	Transmitter Inverted Data Input	3A	
41	Tx6p	CML-I	Transmitter Non-Inverted Data Output	3A	
42	Ground		GND	1A	1
43	Tx8n	CML-I	Transmitter Inverted Data Input	3A	
44	Tx8p	CML-I	Transmitter Non-Inverted Data Output	3A	
45	Ground		GND	1A	1
46	Reserved		For future use	3A	3
47	VS1		Module Vendor Specific1	3A	3
48	VccRx1		3.3V Power Supply	2A	2
49	VS2		Module Vendor Specific2	3A	3
50	VS3		Module Vendor Specific3	3A	3

51	Ground		GND	1A	1
52	Rx7p	CML-O	Receiver Non-Inverted Data Output	3A	
53	Rx7n	CML-O	Receiver Inverted Data Output	3A	
54	Ground		GND	1A	1
55	Rx5p	CML-O	Receiver Non-Inverted Data Output	3A	
56	Rx5n	CML-O	Receiver Inverted Data Output	3A	
57	Ground		GND	1A	1
58	Ground		GND	1A	1
59	Rx6n	CML-O	Receiver Inverted Data Output	3A	
60	Rx6p	CML-O	Receiver Non-Inverted Data Output	3A	
61	Ground		GND	1A	1
62	Rx8n	CML-O	Receiver Inverted Data Output	3A	
63	Rx8p	CML-O	Receiver Non-Inverted Data Output	3A	
64	Ground		GND	1A	1
65	NC		No Connect	3A	3
66	Reseved		For future use	3A	3
67	VccTx1		3.3V Power Supply	2A	2
68	Vcc2		3.3V Power Supply	2A	2
69	ePPS	LVTTL-I	Precision Time Protocol (PTP) reference clock input	3A	3
70	Ground		GND	1A	1
71	Tx7p	CML-I	Transmitter Non-Inverted Data Output	3A	
72	Tx7n	CML-I	Transmitter Inverted Data Output	3A	
73	Ground		GND	1A	1
74	Tx5p	CML-I	Transmitter Non-Inverted Data Output	3A	
75	Tx5n	CML-I	Transmitter Inverted Data Output	3A	
76	Ground		GND	1A	1

Notes:

1. QSFP-DD uses common ground (GND) for all signals and supply (power). All are common within the QSFP-DD module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal common ground plane.

2. VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 shall be applied concurrently. Requirements defined for the host side of the Host Card Edge Connector are listed in Table 6. VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 may be internally connected within the module in any combination. The connector Vcc pins

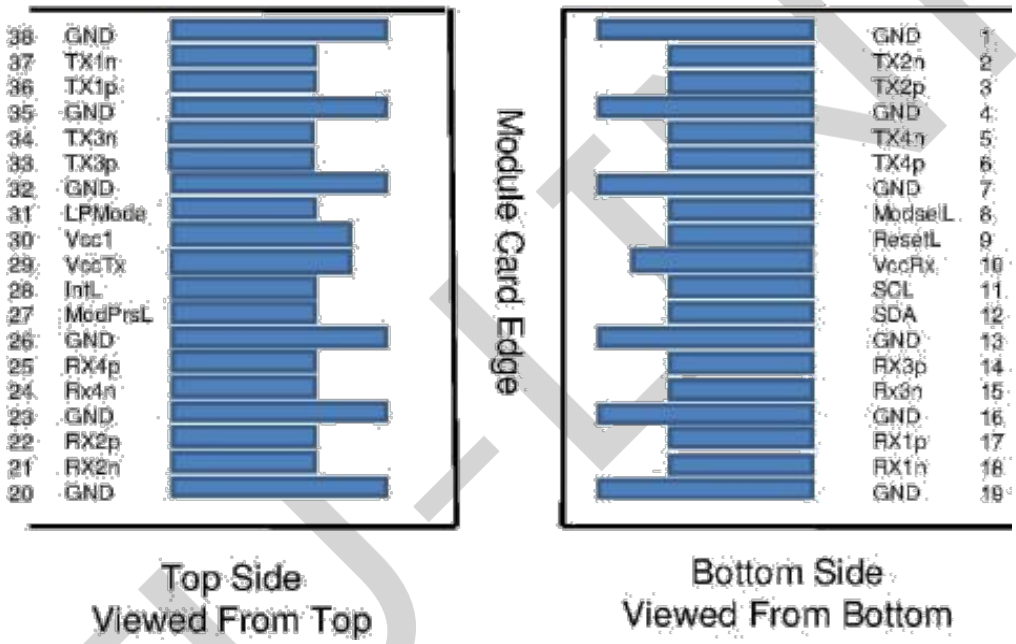
are each rated for a maximum current of 1000 mA.

3. All Vendor Specific, Reserved and No Connect pins may be terminated with 50 ohms to ground on the host. Pad 65 (No Connect) shall be left unconnected within the module. Vendor specific and reserved pads shall have an impedance to GND that is greater than 10Kohms and less than 100pF.

4. Plug Sequence specifies the mating sequence of the host connector and module. The sequence is 1A, 2A, 3A, 1B, 2B, 3B. (see Figure 2 for pad locations) Contact sequence A will make, then break contact with additional QSFP-DD pads. Sequence 1A, 1B

will then occur simultaneously, followed by 2A, 2B, followed by 3A, 3B

QSFP56 end



Pin View for QSFP56

Pin	Symbol	Name/Description	Notes
1	GND	Ground	1
2	Tx2n	Transmitter Inverted Data Input	
3	Tx2p	Transmitter Non-Inverted Data Input	
4	GND	Ground	1
5	Tx4n	NC	2
6	Tx4p	NC	2
7	GND	Ground	1
8	ModSelL	Module Select	
9	ResetL	Module Reset	
10	Vcc Rx	+3.3V Power Supply Receiver	
11	SCL	2-wire serial interface clock	
12	SDA	2-wire serial interface data	

13	GND	Ground	1
14	Rx3p	NC	2
15	Rx3n	NC	2
16	GND	Ground	1
17	Rx1p	Receiver Non-Inverted Data Output	
18	Rx1n	Receiver Inverted Data Output	
19	GND	Ground	1
20	GND	Ground	1
21	Rx2n	Receiver Inverted Data Output	
22	Rx2p	Receiver Non-Inverted Data Output	
23	GND	Ground	1
24	Rx4n	NC	2
25	Rx4p	NC	2
26	GND	Ground	1
27	ModPrsL	Module Present	
28	IntL	Interrupt	
29	Vcc Tx	+3.3V Power supply transmitter	
30	Vcc1	+3.3V Power supply	
31	LPMode	Low Power Mode	
32	GND	Ground	1
33	Tx3p	NC	2
34	Tx3n	NC	2
35	GND	Ground	1
36	Tx1p	Transmitter Non-Inverted Data Input	
37	Tx1n	Transmitter Inverted Data Input	
38	GND	Ground	1

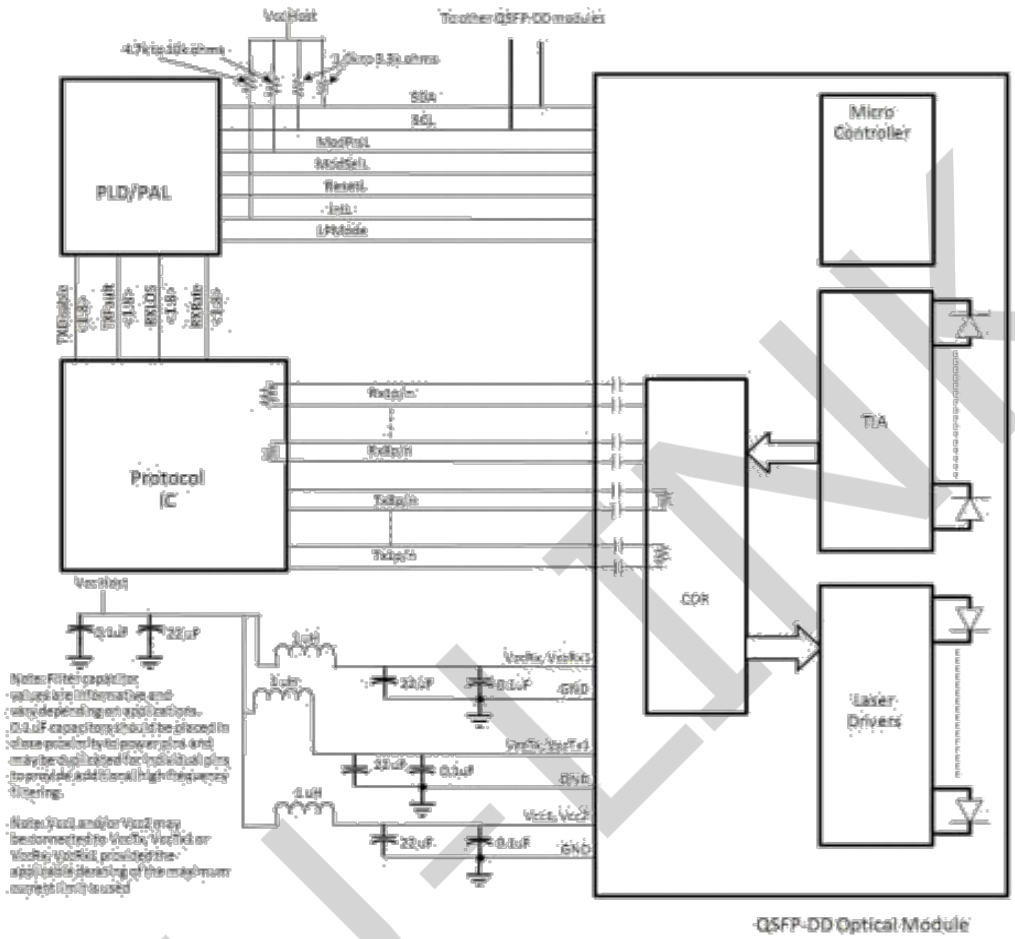
Note 1: GND is the symbol for signal and supply (power) common for the QSFP+ module.

All are common within the QSFP+ module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane

Note 2: Not Connected.

Recommended Interface Circuit

QSFP-DD



QSFP56

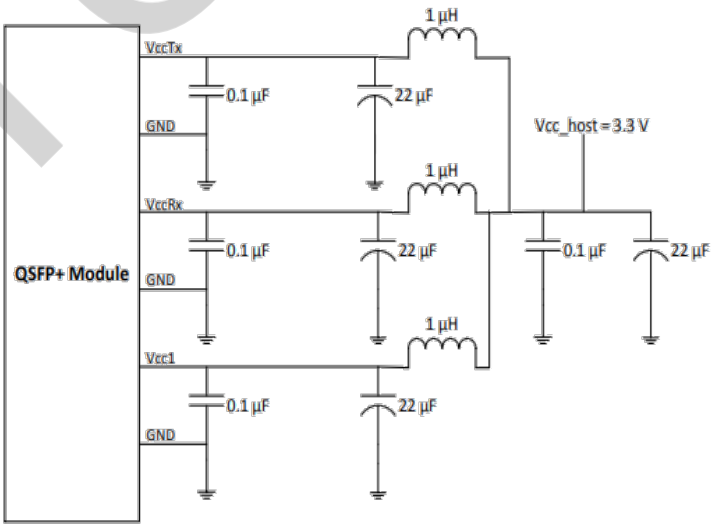
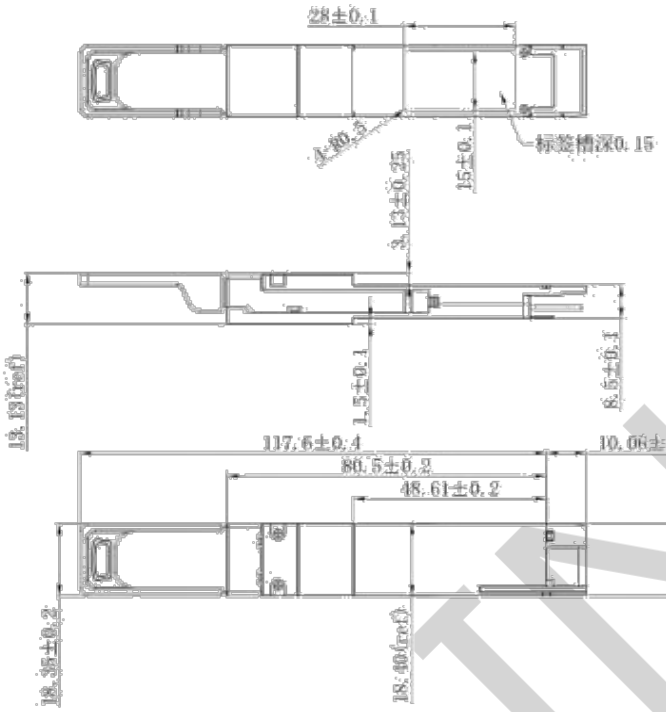
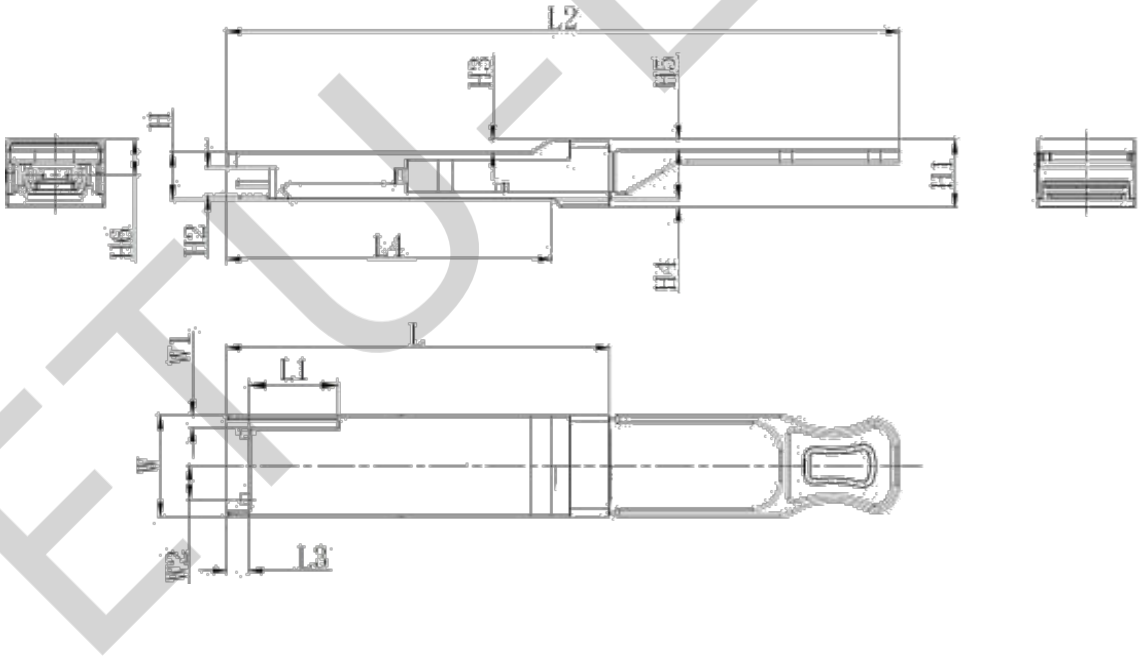


FIGURE 5-4 RECOMMENDED HOST BOARD POWER SUPPLY FILTERING

Mechanical Diagram

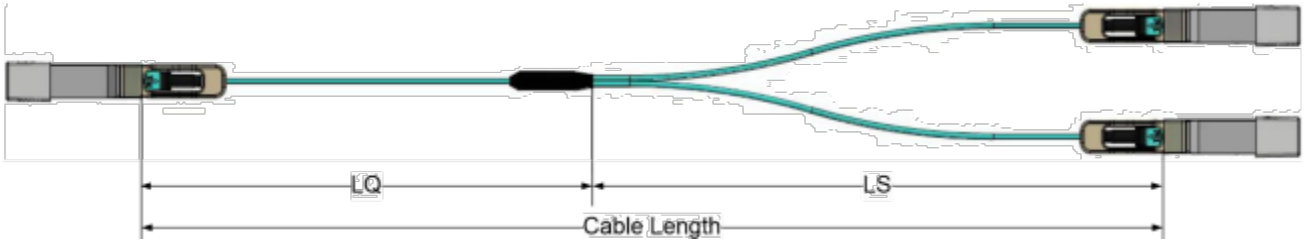


Mechanical Diagram for QSFP-DD



	L	L1	L2	L3	L4	W	W1	W2	H	H1	H2	H3	H4	H5	H6
Max	72.2	-	128	4.35	61.4	18.45	-	6.2	8.6	12.4	5.35	2.5	1.6	2.0	-
Type	72.0	-	-	4.20	61.2	18.35	-	-	8.5	12.2	5.2	2.3	1.5	1.8	6.55
Min	68.8	16.5	124	4.05	61.0	18.25	2.2	5.8	8.4	12.0	5.05	2.1	1.3	1.6	-

Mechanical Diagram for QSFP56



Cable Length

Cable Length（Unit: m）	Tolerant（Unit: cm）
＜1.0	+5/-0
1.0~4.5	+15/-0
5.0~ 14.5	+30/-0
≥15.0	+2%/-0

Cable Nominal Length

Total Length X (Unit: m)	Breakout Point Measured from QSFP LQ (Unit: m)	Breakout Point Measured from SFP LS(Unit: m)
1	0.3	0.7
2	0.6	1.4
3	1	2
5	2	3
7	4	3
10	7	3
15	12	3
20	17	3
25	22	3
30	27	3
40	37	3
50	47	3

Optical Channel Connection

400Gb/s Side	200Gb/s Side
	Port 1
TX1	RX1
RX1	TX1
TX2	RX2
RX2	TX2

TX3	RX3
RX3	TX3
TX4	RX4
RX4	TX4
	Port 2
TX5	RX1
RX5	TX1
TX6	RX2
RX6	TX2
TX7	RX3
RX7	TX3
TX8	RX4
RX8	TX4

Revision History

Version No.	Date	Description
1.0	July 25, 203	Preliminary datasheet
2.0	September 28,2023	Product upgrades

Company: ETU-Link Technology Co., LTD
Production base: Right side of 3rd floor, No. 102 building, Longguan expressway, Dalang street, Longhua District, Shenzhen city, GuangDongProvince,China 518109
R&D base: Floor 4, Building 4, Nanshan Yungu Phase LI, Taoyuan Community, XiliStreet,Nanshan District, Shenzhen
Tel: +86-755 2328 4603

Addresses and phone number also have been listed at www.etulinktechnology.com.
Please e-mail us at sales@etulinktechnology.com or call us for assistance.