

EAQPY-8LCxx

100Gb/s QSFP28 to 8LC Connector Breakout Active Optical Cable

PRODUCT FEATURES

- Transmission data rate up to 25Gbit/s per channel
- Connector1: QSFP28
- Connector2: LC SC ST FC Connector(8)
- Full duplex 4 channel 850nm parallel active optical cable
- Available lengths (in meters):1,2,3,4.....
- SFF-8665 QSFP28 compliant housing and hot pluggable electrical interface
- Differential AC-coupled high speed data interface
- Management Interface and digital diagnostic monitoring
- Commercial temperature range:0 to 70 °C
- Support Rx output pre emphasis
- Housing isolated from connector ground
- Low power consumption
- 3.3V power supply voltage
- RoHS 6 compliant

APPLICATIONS

- 100GBASE SR
- 100G Ethernet
- Proprietary high speed high density data transmission
- Creating a breakout cable with four Duplex LC SC ST FC connectors for port expander applications
- High performance computing server and data storage

Description

100G QSFP28 to 8LC Connector Breakout Active Optical Cable AOC are a high performance low power consumption long reach interconnect solution supporting 100G Ethernet fiber channel and PCIe It is compliant with the QSFP28 MSA. QSFP28 Breakout Cable is an assembly of 4 full-duplex lanes where each lane is capable of transmitting data at rates up to 25Gb /s providing an aggregated rate of 100Gb /s .

QSFP28 Breakout Cable are suitable for short distances and offer a highly cost effective way to connect within racks and across adjacent racks This product is a high data rate parallel active optical cable to overcome the bandwidth limitation of traditional copper cable.

Ordering Information

Part No.	Descriptions
EAQPY-8LCxx-OM3	100G QSFP28 to 8LC Active Optical Cable, Up to 100M,OM3

Notes:

- where "x" denotes cable length in meters. Examples are as follows:
- x = 1 for 1m, xx=10 for 10m

Absolute Maximum Ratings

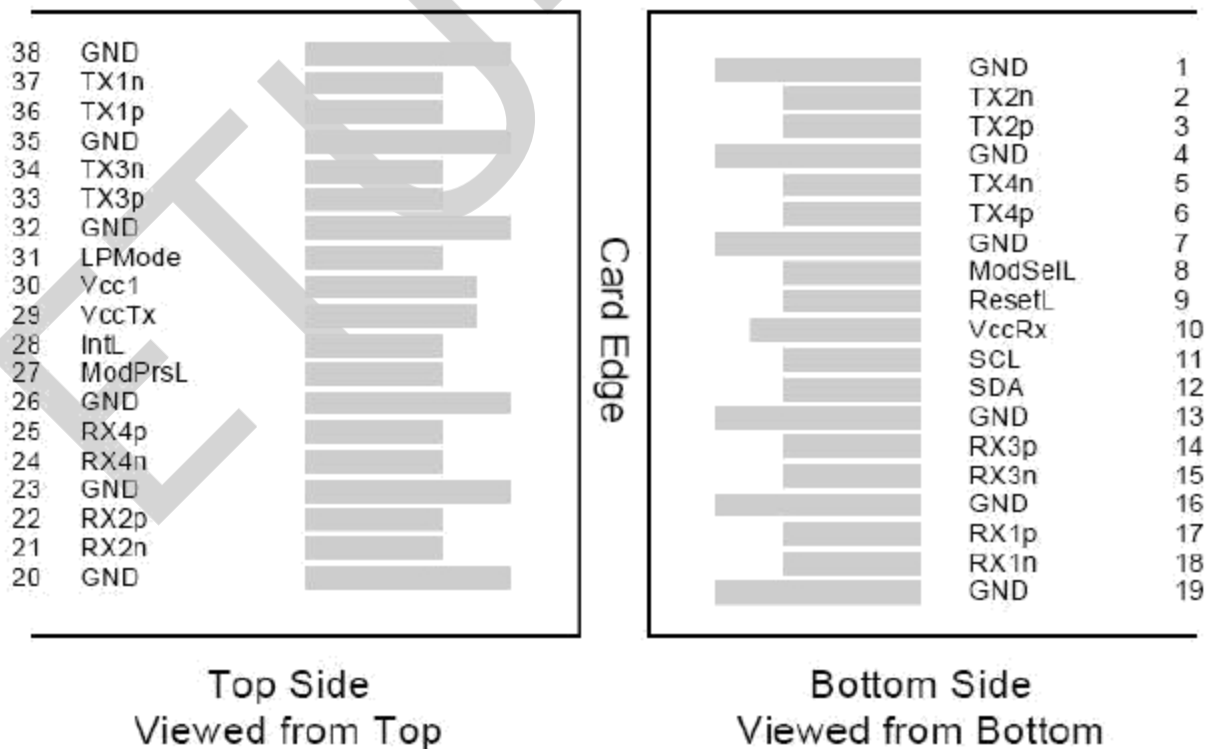
Exceeding the limits below may damage the active optical cable permanently

Parameter	Symbol	Min	Typical	Max	Unit
Operating Case Temperature	TOPC	0		70	□
Power Supply Voltage	VCC	3.13	3.3	3.47	V
Input Voltage	VCC	-0.3		+0.3	V
Power Consumption		-		1.5	W
Data Rate	DR		25.78		G/bps
Link Distance with OM3 fiber	D	0		100	m

Electrical Characteristics

Parameter	Symbol	Min	Typical	Max	Unit
Differential input impedance	Zin	90	100	110	ohm
Differential Output impedance	Zout	90	100	110	ohm
Differential input voltage amplitude	ΔV_{in}	300		1100	mVp-p
Differential output voltage amplitude	ΔV_{out}	500		800	mVp-p
Bit Error Rate	BR			E-12	
Input Logic Level High	V _{IH}	2.0		V _{CC}	V
Input Logic Level Low	V _{IL}	0		0.8	V
Output Logic Level High	V _{OH}	V _{CC} -0.5		V _{CC}	V
Output Logic Level Low	V _{OL}	0		0.4	V

Pin Diagram



Pin Descriptions

PIN	Logic	Symbol	Name/Description	Note
1		GND	Ground	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	
3	CML-I	Tx2p	Transmitter Non-Inverted Data output	
4		GND	Ground	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	
6	CML-I	Tx4p	Transmitter Non-Inverted Data output	
7		GND	Ground	1
8	LVTLL-I	ModSelL	Module Select	
9	LVTLL-I	ResetL	Module Reset	
10		VccRx	+ 3.3V Power Supply Receiver	2
11	LVC MOS-I/O	SCL	2-Wire Serial Interface Clock	
12	LVC MOS-I/O	SDA	2-Wire Serial Interface Data	
13		GND	Ground	
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	
15	CML-O	Rx3n	Receiver Inverted Data Output	
16		GND	Ground	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	
18	CML-O	Rx1n	Receiver Inverted Data Output	
19		GND	Ground	1
20		GND	Ground	1
21	CML-O	Rx2n	Receiver Inverted Data Output	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	

23		GND	Ground	1
24	CML-O	Rx4n	Receiver Inverted Data Output	1
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	
26		GND	Ground	1
27	LVTTL-O	ModPrsL	Module Present	
28	LVTTL-O	IntL	Interrupt	
29		VccTx	+3.3 V Power Supply transmitter	2
30		Vcc1	+3.3 V Power Supply	2
31	LVTTL-I	LPMode	Low Power Mode	
32		GND	Ground	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	
34	CML-I	Tx3n	Transmitter Inverted Data Output	
35		GND	Ground	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	
37	CML-I	Tx1n	Transmitter Inverted Data Output	
38		GND	Ground	1

Notes:

1. Module circuit ground is isolated from module chassis ground within the module. GND is the symbol for signal and supply (power) common for QSFP28 modules.
2. The connector pins are each rated for a maximum current of 500mA.

Low Speed Electrical Hardware Pins

In addition to wire serial interface 100G QSFP28 AOC module has the following low speed pins for control and status

ModSelL Pin

The ModSelL is an input pin. When held low by the host, the module responds to wire serial communication commands. The ModSelL allows the use of multiple QSFP modules on a single wire interface bus. When the ModSelL is “High”, the module will not respond to any wire interface communication from the host. ModSelL has an internal pull up in the module.

ResetL Pin

Reset LPMODE_Reset has an internal pull up in the module. A low level on the ResetL pin for longer than the minimum pulse length $t_{\text{Reset_init}}$ initiates a complete module reset, returning all user module settings to their default state. Module Reset Assert Time t_{init} starts on the rising edge after the low level on the ResetL pin is released. During the execution of a reset t_{init} , the host shall disregard all status bits until the module indicates a completion of the reset interrupt. The module indicates this by posting an IntL signal with the Data_Not_Ready bit negated. Note that on power up, including hot insertion, the module will post this completion of reset interrupt without requiring a reset.

LPMODE Pin

100G QSFP28 AOC operates in the low power mode, less than W power consumption. This pin, active high, will decrease power consumption to less than W.

ModPrsL Pin

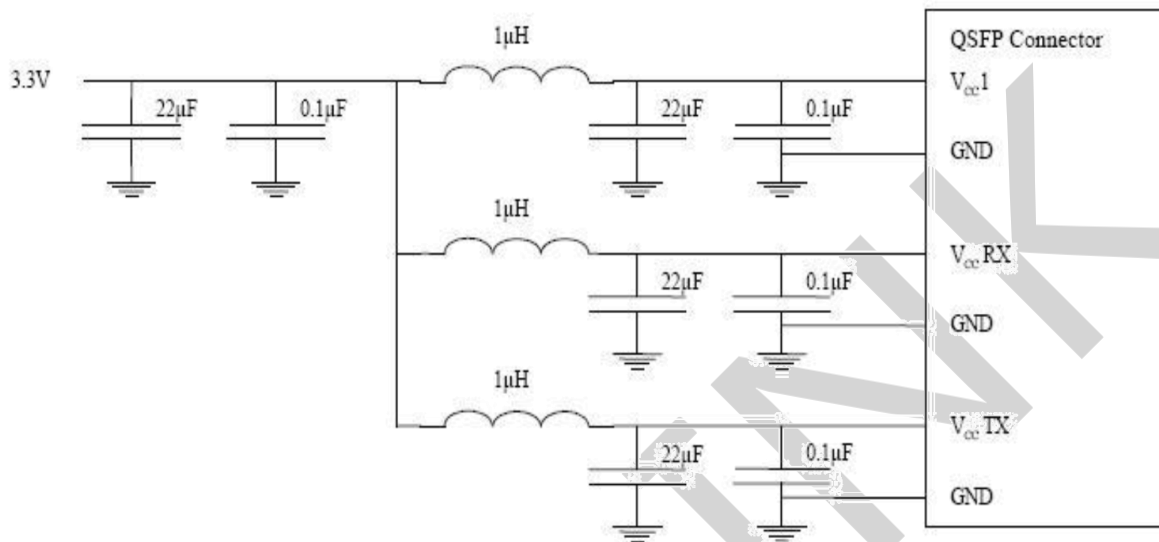
ModPrsL is pulled up to Vcc on the host board and grounded in the module. The ModPrsL is asserted “Low” when the module is inserted and deasserted “High” when the module is physically absent from the host connector.

IntL Pin

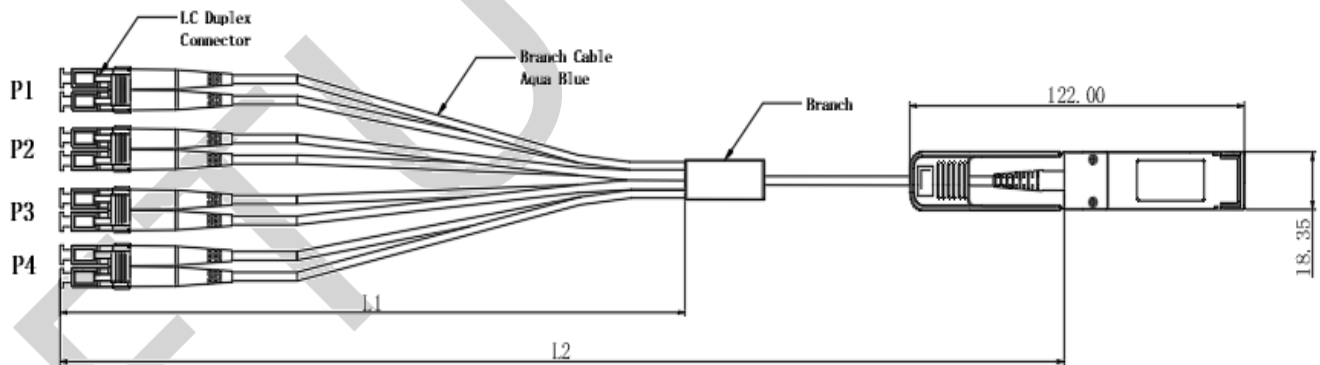
IntL is an output pin. When “Low”, it indicates a possible module operational fault or a status critical to the host system. The host identifies the source of the interrupt by using the wire serial interface. The IntL pin is an open collector output and must be pulled up to Vcc on the host board.

Power Supply Filtering

The host board should use the power supply filtering shown in Figure1.



Mechanical Diagram



Unit: mm

Revision History

Version No.	Date	Description
1.0	May 18, 2019	Preliminary datasheet
1.1	Aug 12, 2024	Product upgrades

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