Rev	Date	Modified by	Description
A0	2023		

Product Specifications

400G OSFP-2x200G QSFP56 Direct Attach Cable (DAC)

PN: EODP40X-32Q5CNxx

Features

- Compatible with IEEE 802.3cd
- Supports aggregate data rates of 2X200Gbps(PAM4)
- Optimized construction to minimize insertion loss and crosstalk
- Pull-to-release slide latch design
- Straight and break out assembly configurations available
- Customized cable braid termination limits EMI radiation
- Customizable EEPROM mapping for cable signature
- 26AWG and 30AWG cable
- 3.3V Power supply
- Temperature Range: 0~ 70 °C
- RoHs Compliant

Applications

- Switches, servers and routers
- Data Center networks
- Storage area networks
- High performance computing
- Telecommunication and wireless infrastructure
- Medical diagnostics and networking
- Test and measurement equipment

Industry Standards

- 2x200G Ethernet(IEEE 802.3cd)
- InfiniBand HDR

Description

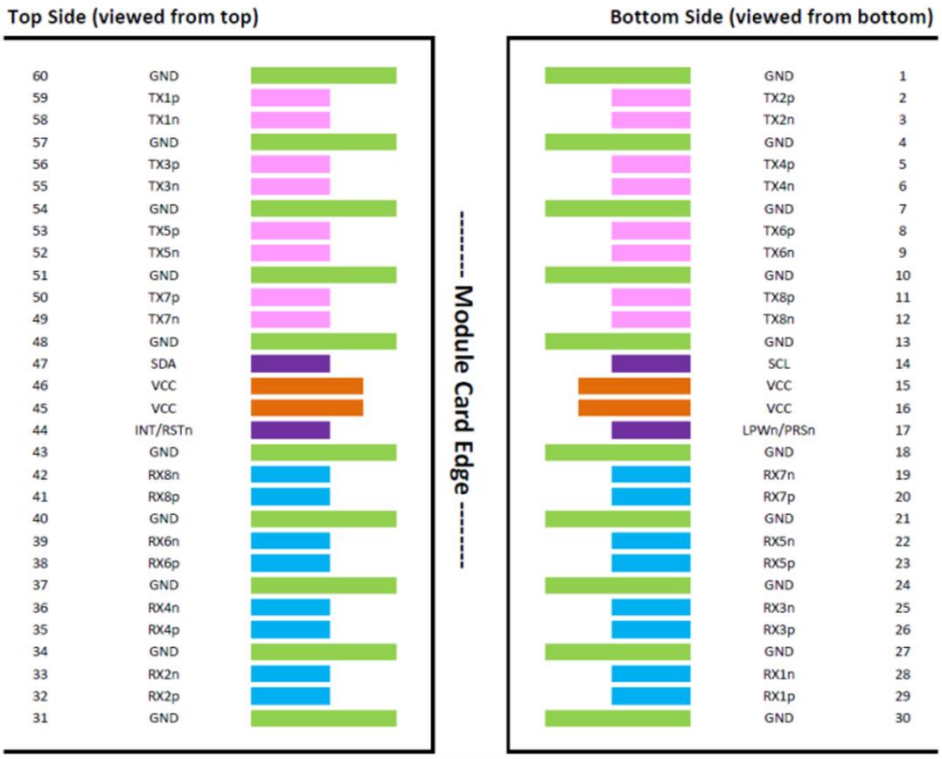
The 400G OSFP_2X200G QSFP56 passive copper cable assembly feature sixteen differential copper pairs, providing eight data transmission channels at speeds up to 56Gbps(PAM4) per channel, and meets 2X200G Ethernet and InfiniBand High Data Rate(HDR) requirements. Available in 26AWG and 30AWG wire gauges, this 400G OSFP_2X200G QSFP56 copper cable assembly features low insertion loss and low crosstalk.
400G OSFP_2X200G QSFP56 passive copper cable uses PAM4 signals for transmission, which doubles the rate. However, there are more stringent requirements for cable insertion loss. For detailed requirements, please see High Speed Characteristics.

Pin Descriptions

OSFP Pin Function Definition

Pin	Logic	Symbol	Description
1		GND	Ground
2	CML-I	Tx2p	Transmitter Non-Inverted Data Input
3	CML-I	Tx2n	Transmitter Inverted Data Input
4		GND	Ground
5	CML-I	Tx4p	Transmitter Non-Inverted Data Input
6	CML-I	Tx4n	Transmitter Inverted Data Input
7		GND	Ground
8	CML-I	Tx6p	Transmitter Non-Inverted Data Input
9	CML-I	Tx6n	Transmitter Inverted Data Input
10		GND	Ground
11	CML-I	Tx6p	Transmitter Non-Inverted Data Input
12	CML-I	Tx6n	Transmitter Inverted Data Input
13		GND	Ground
14	LVCMOS-I/O	SCL	2-wire serial interface clock
15		VCC	+3.3V Power supply
16		VCC	+3.3V Power supply
17		LPWn/PRSn	Low-Power Mode / Module Present
18		GND	Ground
19	CML-O	Rx7n	Receiver Inverted Data Output
20	CML-O	Rx7p	Receiver Non-Inverted Data Output
21		GND	Ground
22	CML-O	Rx5n	Receiver Inverted Data Output
23	CML-O	Rx5p	Receiver Non-Inverted Data Output
24		GND	Ground
25	CML-O	Rx3n	Receiver Inverted Data Output
26	CML-O	Rx3p	Receiver Non-Inverted Data Output

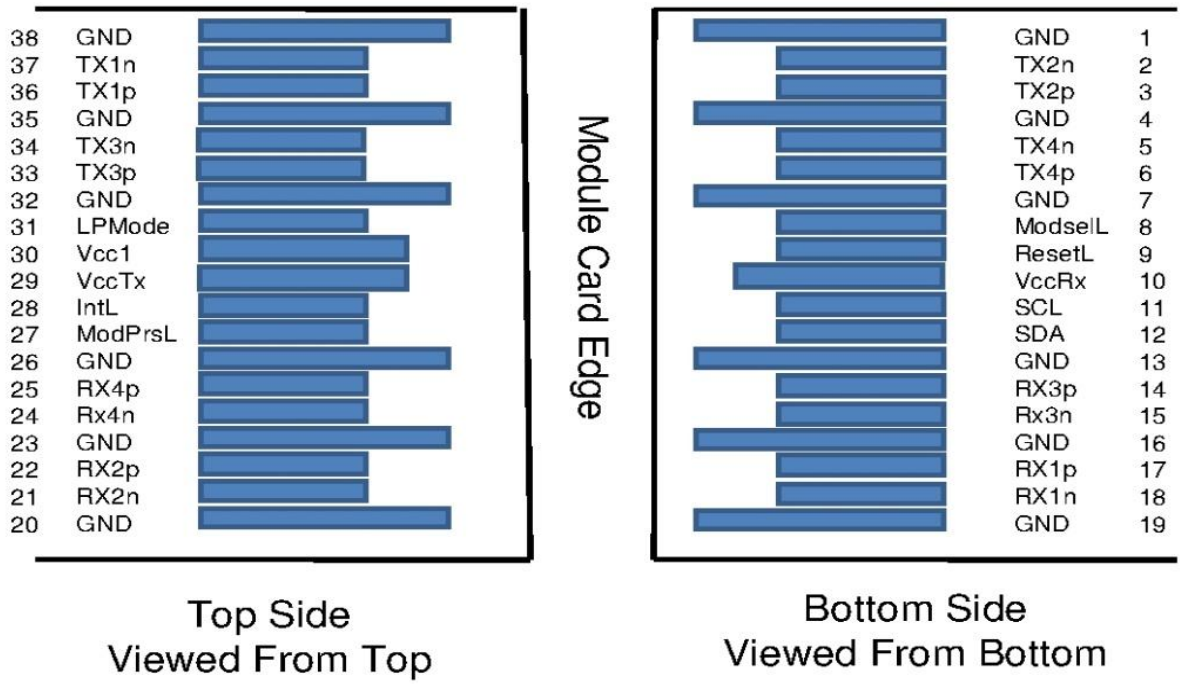
27		GND	Ground
28	CML-O	Rx1n	Receiver Inverted Data Output
29	CML-O	Rx1p	Receiver Non-Inverted Data Output
30		GND	Ground
31		GND	Ground
32	CML-O	Rx2p	Receiver Non-Inverted Data Output
33	CML-O	Rx2n	Receiver Inverted Data Output
34		GND	Ground
35	CML-O	Rx4p	Receiver Non-Inverted Data Output
36	CML-O	Rx4n	Receiver Inverted Data Output
37		GND	Ground
38	CML-O	Rx6p	Receiver Non-Inverted Data Output
39	CML-O	Rx6n	Receiver Inverted Data Output
40		GND	Ground
41	CML-O	Rx8p	Receiver Non-Inverted Data Output
42	CML-O	Rx8n	Receiver Inverted Data Output
43		GND	Ground
44		INT/RSTn	Module Interrupt / Module Reset
45		VCC	+3.3V Power supply
46		VCC	+3.3V Power supply
47	LVCMOS-I/O	SDA	2-wire serial interface data
48		GND	Ground
49	CML-I	Tx7n	Transmitter Inverted Data
50	CML-I	Tx7p	Input Transmitter Non-Inverted Data Input
51		GND	Ground
52	CML-I	Tx5n	Transmitter Inverted Data
53	CML-I	Tx5p	Input Transmitter Non-Inverted Data Input
54		GND	Ground
55	CML-I	Tx3n	Transmitter Inverted Data
56	CML-I	Tx3p	Input Transmitter Non-Inverted Data Input
57		GND	Ground
58	CML-I	Tx1n	Transmitter Inverted Data
59	CML-I	Tx1p	Input Transmitter Non-Inverted Data Input
60		GND	Ground



QSFP56 Pin Function Definition

Pin	Logic	Symbol	Description
1		GND	Ground
2	CML-I	Tx2n	Transmitter Inverted Data Input
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input
4		GND	Ground
5	CML-I	Tx4n	Transmitter Inverted Data Input
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input
7		GND	Ground
8	LVTTL-I	ModSelL	Module Select
9	LVTTL-I	ResetL	Module Reset
10		Vcc Rx	+3.3V Power Supply Receiver
11	LVCMOS- I/O	SCL	2-wire serial interface clock
12	LVCMOS- I/O	SDA	2-wire serial interface data
13		GND	Ground
14	CML-O	Rx3p	Receiver Non-Inverted Data Output
15	CML-O	Rx3n	Receiver Inverted Data Output
16		GND	Ground
17	CML-O	Rx1p	Receiver Non-Inverted Data Output
18	CML-O	Rx1n	Receiver Inverted Data Output

19		GND	Ground
20		GND	Ground
21	CML-O	Rx2n	Receiver Inverted Data Output
22	CML-O	Rx2p	Receiver Non-Inverted Data Output
23		GND	Ground
24	CML-O	Rx4n	Receiver Inverted Data Output
25	CML-O	Rx4p	Receiver Non-Inverted Data Output
26		GND	Ground
27	LVTTL-O	ModPrsL	Module Present
28	LVTTL-O	IntL	Interrupt
29		Vcc Tx	+3.3V Power supply transmitter
30		Vcc1	+3.3V Power supply
31	LVTTL-I	LPMode	Low Power Mode
32		GND	Ground
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input
34	CML-I	Tx3n	Transmitter Inverted Data Input
35		GND	Ground
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input
37	CML-I	Tx1n	Transmitter Inverted Data Input
38		GND	Ground



Top Side
Viewed From Top

Bottom Side
Viewed From Bottom

General Product Characteristics

OSFP_2XQSFP56 DAC Specifications	
Number of Lanes	Tx8 & Rx8(400G OSFP) Tx4 & Rx4(2X200G QSFP56)
Channel Data Rate	53.125Gbps
Operating Temperature	0 to + 70°C
Storage Temperature	-40 to + 85°C
Supply Voltage	3.3 V nominal
Electrical Interface	60pins edge connector(OSFP) 38pins edge connector(QSFP56)
Management Interface	Serial, I^2C

High Speed Characteristics

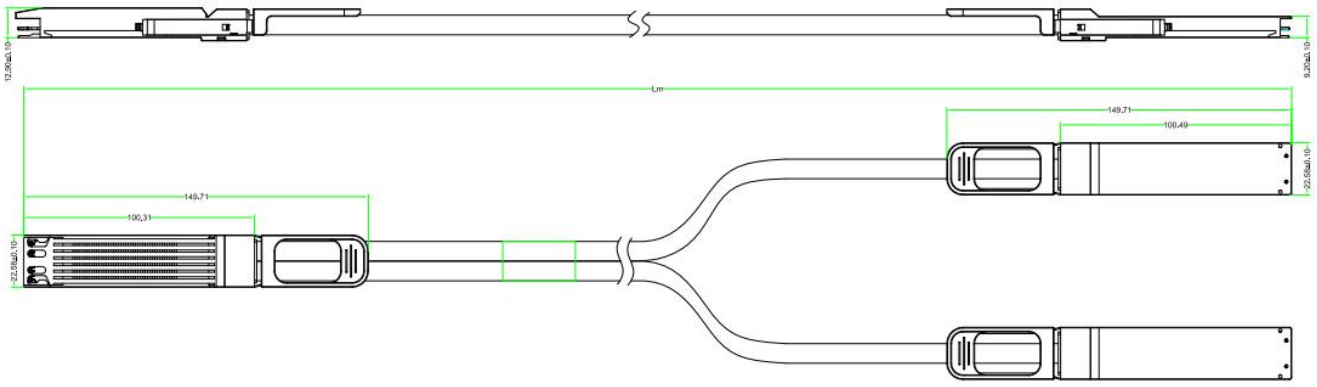
Parameter	Symbol	Min	Typical	Max	Unit	Note
Differential Impedance	TDR	90	100	110	Ω	
Insertion loss	SDD21	-17.16			dB	At 13.28 GHz
Differential Return Loss	SDD11 SDD22			See 1	dB	At 0.05 to 4.1 GHz
				See 2	dB	At 4.1 to 19 GHz
Common-mode to common-mode output return loss	SCC11 SCC22			-2	dB	At 0.2 to 19 GHz
Differential to common-mode return loss	SCD11 SCD22			See 3	dB	At 0.01 to 12.89 GHz
				See 4		At 12.89 to 19 GHz
Differential to common Mode Conversion Loss	SCD21-IL			-10	dB	At 0.01 to 12.89 GHz
				See 5		At 12.89 to 15.7 GHz
				-6.3		At 15.7 to 19 GHz

Notes:

1. Reflection Coefficient given by equation SDD11(dB) < -16.5 + 2 × SQRT(f), with f in GHz
2. Reflection Coefficient given by equation SDD11(dB) < -10.66 + 14 × log10(f/5.5), with f in GHz
3. Reflection Coefficient given by equation SCD11(dB) < -22 + (20/25.78)*f, with f in GHz
4. Reflection Coefficient given by equation SCD11(dB) < -15 + (6/25.78)*f, with f in GHz
5. Reflection Coefficient given by equation SCD21(dB) < -27 + (29/22)*f, with f in GHz

Mechanical Specifications

The connector is compatible with the SFF8024 (OSFP) and SFF8672 (QSFP56) specification.



Length (m)	Cable AWG
1	30
1.5	30
2	26

Regulatory Compliance

Feature	Test Method	Performance
Electrostatic Discharge (ESD) to the Electrical Pins	MIL-STD-883C Method 3015.7	Class 1(>2000 Volts)
Electromagnetic Interference(EMI)	FCC Class B CENELEC EN55022 Class B CISPR22 ITE Class B	Compliant with Standards
RF Immunity(RFI)	IEC61000-4-3	Typically Show no Measurable Effect from a 10V/m Field Swept from 80
RoHS Compliance	RoHS Directive 2011/65/EU and it's Amendment Directives （EU）2015/863	RoHS （EU）2015/863 compliant
REACH Compliance	REACH Regulation (EC) No 1907/2006	REACH (EC) No 1907/2006 compliant

Company: ETU-Link Technology Co., LTD
Address: Right side of 3rd floor, No. 102 building, Longguan expressway, Dalang street, Longhua District, Shenzhen city, GuangDongProvince,China 518109
Tel: +86-755 2328 4603

Addresses and phone number also have been listed at www.etulinktechnology.com.
Please e-mail us at sales@etulinktechnology.com or call us for assistance.