EQD400-SR8

400G QSFP-DD SR8 100m Optical Transceiver

PRODUCT FEATURES

- QSFP-DD MSA compliant
- QSFP-DD CMIS4.0 management interface compliant
- IEEE 802.3cm 400GBASE-SR8 standard compliant
- IEEE 802.3bs 400GAUI-8 standard compliant
- Digital diagnostic functions
- 8-channel full-duplex transceiver module
- 425 Gbps aggregate bit rate
- Maximum link length of 70 m OM3, 100 m OM4 with FEC
- Single MPO-16/APC receptacle
- Maximum power dissipation < 10 W
- Operating case temperature range 0°C to 70°C
- Single 3.3 V power supply
- RoHS 2 compliant

APPLICATIONS

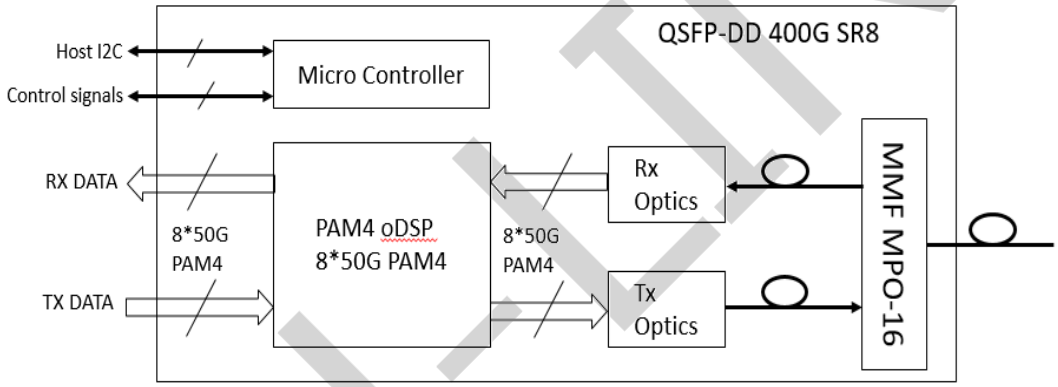
- 400G Ethernet
- Data center network

DESCRIPTIONS

This is a parallel 400GE Quad Small Form Factor Pluggable Double Density (QSFP-DD) SR8 optical module designed for optical communication applications. The optical module uses a 4-level pulse amplitude modulation (PAM4) format. The optical module provides point-to-point 400 Gigabit Ethernet links over eight pairs of multimode fiber, with a reach of up to 100 m for OM4 (MMF) and 70 m for OM3 (MMF).

It is compliant with QSFP-DD MSA standard and IEEE 802.3cm 400GBASE-SR8 standard and IEEE 802.3bs 400GAUI-8 standard. Digital diagnostics functions are available via the I2C interface, as specified by the QSFP-DD MSA.

Module Block Diagram



Ordering Information

Part No.	Description
EQD400-SR8	400G QSFP-DD SR8 100m Optical Transceiver MPO-16/APC

Absolute Maximum Ratings

It has to be noted that the operation in excess of any individual absolute maximum ratings might cause permanent damage to this module.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Maximum supply voltage	Vcc	–0.5	3.3	3.6	V	
Storage temperature	Ts	–40		85	°C	
Relative humidity	RH	5		85	%	Non-condensing
Damage threshold, each lane	THd	5			dBm	

Recommended Operating Conditions

Electrical and optical characteristics below are defined under this operating environment, unless otherwise specified.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Supply voltage	Vcc	3.135	3.3	3.465	V	
Case temperature	Tc	0		70	°C	
Data rate, each lane			26.5625		GBd	
Data rate accuracy		–100		100	ppm	
Modulation format		PAM4				
Link distance with OM3 MMF				70	m	
Link distance with OM4 MMF				100	m	
Link distance with OM5 MMF				100	m	

Note:

Initialization Flows: The Host Initialization Flows of CMIS Rev4.0 Standard Appendix C are recommended.

Electrical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Power dissipation				10	W	
Steady state current	Icc			3189	mA	1
Instantaneous peak current				4000	mA	
Sustained peak current				3300	mA	
Module-to-Host electrical specifications at TP4 (module output)						
Differential voltage pk-pk	Vpp			900	mV	
Common mode voltage	Vcm	–350		2850	mV	2
AC common-mode output voltage (RMS)				17.5	mV	
Transition time	Trise/Tfall	9.5			ps	20%~80%
Differential termination resistance mismatch				10	%	
Near-end ESMW (eye symmetry mask width)		0.265			UI	
Near-end eye height, differential		70			mV	
Far-end ESMW (eye symmetry mask width)		0.20			UI	
Far-end eye height, differential		30			mV	
Far-end pre-cursor ISI ratio		–4.5		2.5	%	

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Differential output return loss		IEEE 802.3-2018 Equation (83E-2)			dB	
Common to differential mode conversion return loss		IEEE 802.3-2018 Equation (83E-3)			dB	
Host-to-Module electrical specifications (module input)						
Differential termination resistance mismatch				10	%	
Overload differential voltage pk-pk	Vpp	900			mV	TP1a
DC common mode voltage	Vcm	–350		2850	mV	TP1
Single-ended voltage tolerance		–0.4		3.3	V	TP1a
Module stressed input test		IEEE 802.3bs 120E.3.4.1				TP1a
Differential input return loss		IEEE 802.3-2018 Equation (83E-5)			dB	TP1
Differential to common mode input return loss		IEEE 802.3-2018 Equation (83E-6)			dB	TP1

Note:

1.The module must stay within its declared power class.

2.DC common mode voltage is generated by the host. Specification includes effects of ground offset voltage.

Optical and Characteristics

Parameters	Symbol	Min.	Typ.	Max.	Unit	Notes
Center wavelength	λ_c	840		860	nm	
Transmitter						
RMS spectral width				0.6	nm	
Average launch power, each lane	P_{AVG}	–6.5		4	dBm	
Outer optical modulation amplitude (OMA_{outer}), each lane	P_{OMA}	–4.5		3	dBm	
Launch power in OMA_{outer} minus TDECQ, each lane		–5.9			dBm	
Transmitter and dispersion eye closure for PAM4, each lane	TDECQ			4.5	dB	
TDECQ – $10\log_{10}(C_{eq})$, each lane				4.5	dB	
Extinction ratio, each lane	ER	3			dB	
Transmitter transition time, each lane				34	ps	
Average launch power of OFF transmitter, each lane	P_{OFF}			–30	dBm	
$RIN_{12}OMA$				–128	dB/Hz	

Parameters	Symbol	Min.	Typ.	Max.	Unit	Notes
Optical return loss tolerance				12	dB	
Encircled flux		≥ 86% at 19 μm ≤ 30% at 4.5 μm				
Receiver						
Average receiver power, each lane		–8.4		4	dBm	
Receiver power, each lane (OMA)				3	dBm	
Damage threshold, each lane	THd	5			dBm	
Receiver reflectance				–12	dB	
LOS assert	LosA	–24.6			dBm	
LOS de-assert	LosD			–8	dBm	
LOS hysteresis	LosH	0.5			dB	
Receiver sensitivity (OMA $_{outer}$), each lane	Sen			Max (–6.5, SECQ – 7.9)	dB	
Stressed receiver sensitivity (OMA), each lane	SRS			–3.4	dBm	
Conditions of stressed receiver sensitivity test						
Stressed eye closure for PAM4, lane under test	SECQ			4.5	dB	
SECQ – 10log$_{10}$ (C_{eq}), lane under test				4.5	dB	
OMA $_{outer}$ of each aggressor lane				3	dBm	

EEPROM Definitions

Refer to CMIS Rev4.0 used for QSFP-DD.

Digital Diagnostics

Digital Diagnostic Management Interface (DDMI) is realized by I2C interface in compliance with CMIS 4.0. diagnostic management functions are realized, and the data addresses are listed in the form below.

Performance Item	Related Bytes	Monitor Error	Notes
Module temperature	Lower Page (14 to 15)	≤ ±3°C	1, 2
Module voltage	Lower Page (16 to 17)	≤ ±3%	2
Transmitter optical power	Upper Page11h (154 to 169)	≤ ±3 dB	2
Bias current	Upper Page11h (170 to 185)	≤ ±10%	2
Receiver optical power	Upper Page11h (186 to 201)	≤ ±3 dB	2

Note:

1.Actual temperature test point is fixed on module case around laser array.

2.Full operating temperature range.

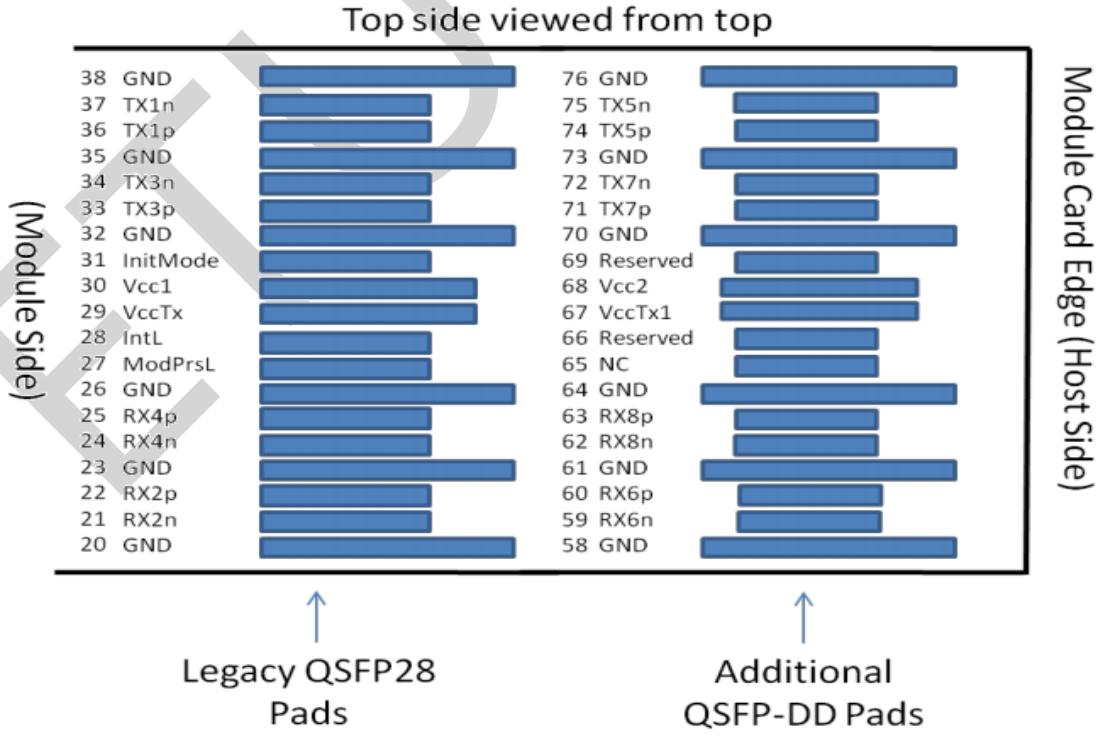
Alarm and Warning Thresholds

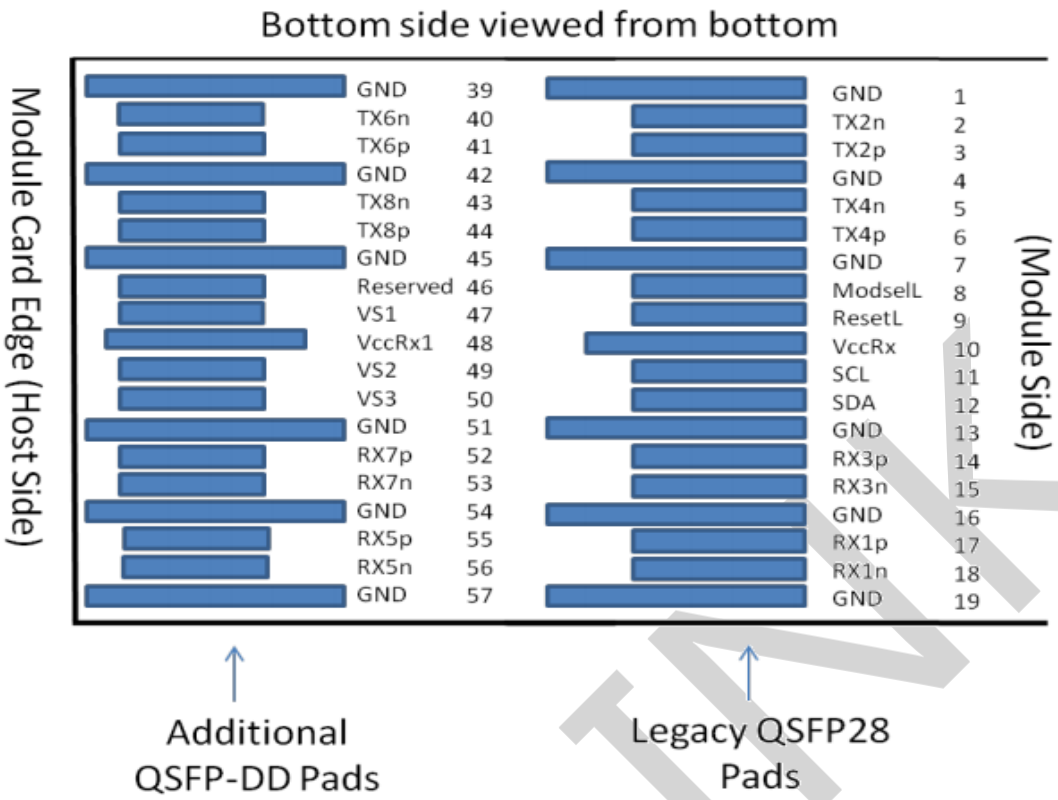
It supports alarms function, indicating the values of the preceding basic performance are lower or higher than the thresholds.

Performance Item	Alarm Threshold Bytes (Page02h Memory)	Unit	Low Threshold	High Threshold
Temperature warning	132 to 135	°C	0	70
Voltage warning	140 to 143	V	3.135	3.465
Ibias warning	188 to 191	mA	5	8.5
Tx power warning	180 to 183	dBm	–6.5	5.5
Rx power warning	196 to 199	dBm	–7	5.5
Temperature alarm	128 to 131	°C	–10	80
Voltage alarm	136 to 139	V	2.97	3.63
Ibias alarm	184 to 187	mA	4	9.5
Tx power alarm	176 to 179	dBm	–9.5	7
Rx power alarm	192 to 195	dBm	–10	7

Pin Diagram

The QSFP-DD SR8 module edge connector consists of a single paddle card with 38 pads on the top and 38 pads on the bottom for a total of 76 pads. The pads are defined in such a manner so as to accommodate insertion of a QSFP module into a QSFP-DD receptacle.





Pin Definitions

Pin	Logic	Symbol	Description	Notes
1		GND	Ground	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	
4		GND	Ground	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	
7		GND	Ground	1
8	LVTTL-I	ModSelL	Module Select	
9	LVTTL-I	ResetL	Module Reset	
10		VccRx	+3.3 V Power Supply	2
11	LVCMOS-I/O	SCL	2-wire Serial Interface Clock	
12	LVCMOS-I/O	SDA	2-wire Serial Interface Data	
13		GND	Ground	1
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	
15	CML-O	Rx3n	Receiver Inverted Data Output	
16		GND	Ground	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	
18	CML-O	Rx1n	Receiver Inverted Data Output	
19		GND	Ground	1
20		GND	Ground	1

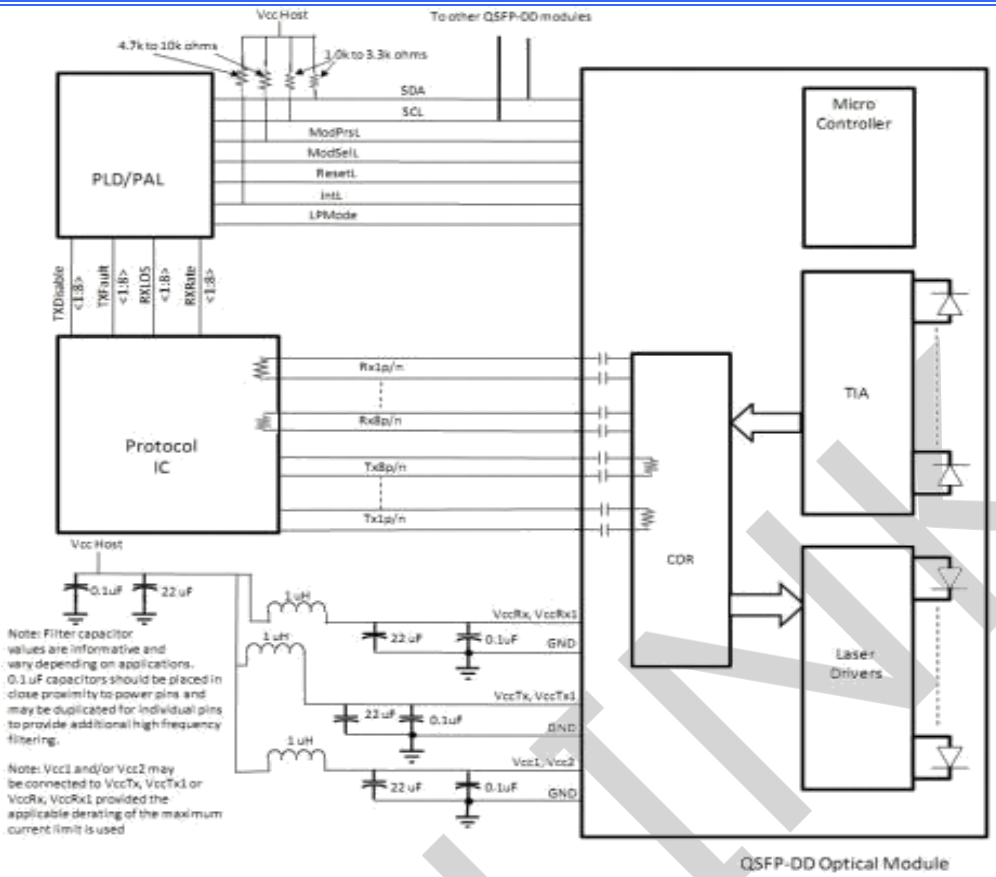
Pin	Logic	Symbol	Description	Notes
21	CML-O	Rx2n	Receiver Inverted Data Output	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	
23		GND	Ground	1
24	CML-O	Rx4n	Receiver Inverted Data Output	
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	
26		GND	Ground	1
27	LVTTL-O	ModPrsL	Module Present	
28	LVTTL-O	IntL	Interrupt	
29		VccTx	+3.3 V Power Supply	2
30		Vcc1	+3.3 V Power Supply	2
31	LVTTL-I	LPMode	Low Power Mode	
32		GND	Ground	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	
34	CML-I	Tx3n	Transmitter Inverted Data Input	
35		GND	Ground	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	
37	CML-I	Tx1n	Transmitter Inverted Data Input	
38		GND	Ground	1
39		GND	Ground	1
40	CML-I	Tx6n	Transmitter Inverted Data Input	
41	CML-I	Tx6p	Transmitter Non-Inverted Data Input	
42		GND	Ground	1
43	CML-I	Tx8n	Transmitter Inverted Data Input	
44	CML-I	Tx8p	Transmitter Non-Inverted Data Input	
45		GND	Ground	1
46		Reserved	For Future Use, No Connect	
47		VS1	Module Vendor Specific 1, No Connect	
48		VccRx1	+3.3 V Power Supply	2
49		VS2	Module Vendor Specific 2	
50		VS3	Module Vendor Specific 3	
51		GND	Ground	1
52	CML-O	Rx7p	Receiver Non-Inverted Data Output	
53	CML-O	Rx7n	Receiver Inverted Data Output	
54		GND	Ground	1
55	CML-O	Rx5p	Receiver Non-Inverted Data Output	
56	CML-O	Rx5n	Receiver Inverted Data Output	
57		GND	Ground	1
58		GND	Ground	1
59	CML-O	Rx6n	Receiver Inverted Data Output	
60	CML-O	Rx6p	Receiver Non-Inverted Data Output	
61		GND	Ground	1
62	CML-O	Rx8n	Receiver Inverted Data Output	

Pin	Logic	Symbol	Description	Notes
63	CML-O	Rx8p	Receiver Non-Inverted Data Output	
64		GND	Ground	1
65		NC	No Connect	
66		Reserved	For Future Use, No Connect	
67		VccTx1	+3.3 V Power Supply	2
68		Vcc2	+3.3 V Power Supply	2
69		Reserved	For Future Use, No Connect	
70		GND	Ground	1
71	CML-I	Tx7p	Transmitter Non-Inverted Data Input	
72	CML-I	Tx7n	Transmitter Inverted Data Input	
73		GND	Ground	1
74	CML-I	Tx5p	Transmitter Non-Inverted Data Input	
75	CML-I	Tx5n	Transmitter Inverted Data Input	
76		GND	Ground	1

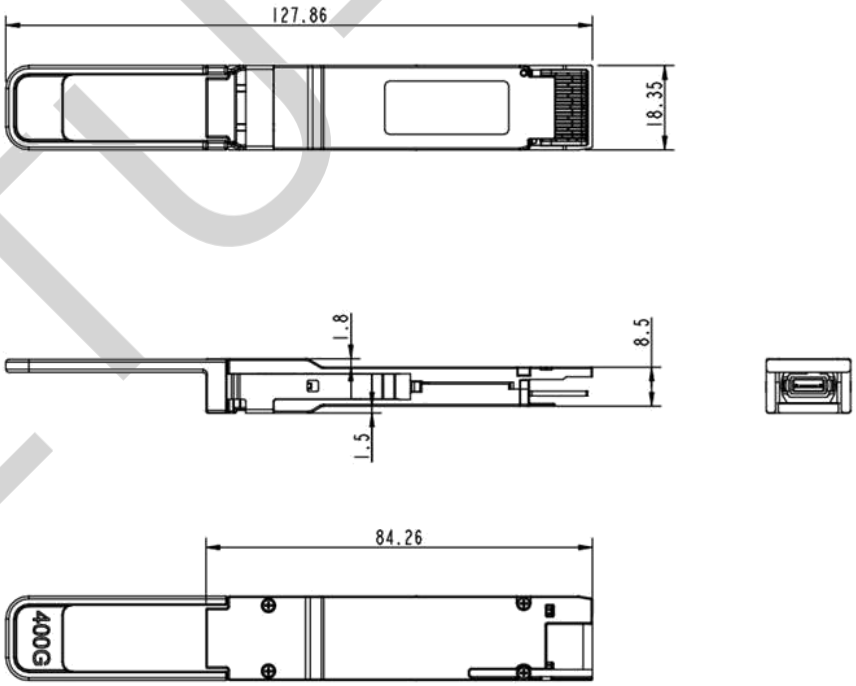
Note:

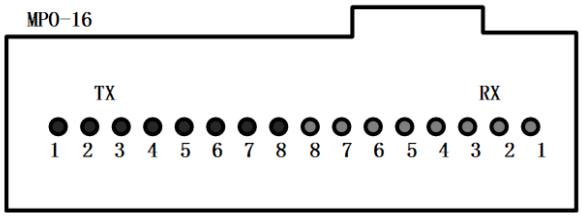
1. 1.QSFP-DD uses common ground (GND) for all signals and supply (power). All are common within the QSFP-DD module and all module voltages are referred to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane.
2. 2.VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 shall be applied concurrently. VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 may be internally connected within the module in any combination. Each connector Vcc pin is rated for a maximum current of 1000 mA.

Recommended Interface Circuit



Mechanical Diagram





Note:

The module uses MPO-16 APC receptacle. It may need every optical connector of the transmission link with APC interface for lower optical reflectance.

Optical Interface

The QSFP-DD 400GE SR8 optical interface port shall be a male MPO-16 APC receptacle. The recommended location and numbering of the optical ports for each of the media dependent interfaces is shown in 错误!未找到引用源。. The transmitter and receiver optical lanes shall occupy the positions depicted in when looking into the MDI receptacle with the connector keyway feature on top.

Revision History

Version No.	Date	Description
1.0	February 18, 2022	Preliminary datasheet
2.0	Sep 13,2024	Format change

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