EQD400-eDR4

400G QSFP-DD eDR4 Optical Transceiver

PRODUCT FEATURES

- Compliant with QSFP-DD MSA and CMIS Rev 4
- Compliant with 802.3bs: 400GAUI-8 Electrical Interface
- Compliant with IEEE802.3cu: 4x100GBASE-FR1 Optical Interface
- Lane bit rate 106.25 Gb/s with PAM4
- Maximum link length of 10km G.652 SMF with KP4-FEC
- Single +3.3V power supply
- Case temperature range: 0 ~ +70℃
- Maximum power consumption:10W
- MPO-12 Optical Receptacle
- RoHS compliant

APPLICATIONS

- 400G BASE-DR4
- Data Center Interconnect
- Enterprise Networking

Description

ETU-LINK's EQD400-eDR4 is a 400Gb/s QSFP-DD optical module designed for 10KM optical communication applications. It is compliant to QSFP-DD MSA, IEEE 802.3bs 400GBASE-DR4 protocol and 400GAUI-8 standard. The 425-Gigabit signal is carried over four parallel lanes by one wavelength per lane. This module can convert 8 channels of 53.125 Gbit/s electrical data to 4 parallel channels of optical signals, each supporting 106.25 Gbit/s data transmission. Reversely, it can convert 4 channels of 106.25 Gbit/s optical signals to 8 channels of electrical output data on the receiver side. It is designed to meet the harshest external operating conditions including temperature, humidity and EMI interference. The module offers very high functionality and feature integration, accessible via a two-wire serial interface.

Ordering information

Part No.	Data Rate	Laser	Fiber Type	Distance	Optical Interface	Temp	DDMI
EQD400-eDR4	400Gbps	EML	SMF	10KM	MPO	0~70C	Y

I、Recommend Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Operating Case Temperature	TOP	0		70	degC	
Power Supply Voltage	VCC	3.14	3.3	3.46	V	
Lane Bit Rate			53.125		GBd	With PAM4
Power Consumption	P_D			10	W	
Pre-FEC Bit Error Ratio				$2.4x10^{-4}$		
Link Distance with G.652	TD			10	KM	

II、Absolute Maximum Ratings

It has to be noted that the operation in excess of any individual absolute maximum ratings might cause permanent damage to this module.

Parameter	Symbol	Min.	Typical	Max.	Unit	Notes
Storage Temperature	T_S	-40	-	+85	°C	
Supply Voltage	V_{CC}	-0.5	-	+4.0	V	
Operating Relative Humidity	RH	-	-	+85	%	

III、Optical Characteristics

Parameter	Symbol	Min.	Typical	Max.	Unit	Notes
Transmitter						
Center Wavelength	λ_c	1304.5	1310	1317.5	nm	
Average Launch Power per Lane	P_{AVG}	-2.7		5.1	dBm	1
Outer Optical Modulation Amplitude (OMAouter), each lane	P_{OMA}	-0.3		4.4	dBm	2
Launch power in OMA_{outer} minus TDECQ, per lane		-2.2			dB	ER≧5 dB
		-1.9			dB	ER<5dB
Transmitter and dispersion eye closure for PAM4 (TDECQ), per lane	TDECQ			3.4	dB	
Difference in launch power between any two lanes (OMA_{outer})	$P_{TX\_DELTA\_LANE}$			4.6	dB	
Average Output Power (Laser Turn off)	$P_{0UT-OFF}$			-16	dBm	
Side Mode Suppression Ratio	SMSR	30			dB	
Extinction Ratio	ER	3.5			dB	
Optical Return Loss Tolerance				15.6	dB	
Transmitter Reflectance				-26	dB	
Receiver						
Center Wavelength	λ_c	1304.5	1310	1317.5	nm	
Damage threshold, per lane	Pdamage	5			dBm	3
Average Rx Power per Lane	P_{RX_LANE}	-9		5.1	dBm	4
Difference in receive power between any two lanes (OMA_{outer})	$P_{RX\_DELTA\_LANE}$			6.1	dB	
Receiver power (OMA_{outer}), each lane	$P_{OMAouter\_LANE}$			4.4	dBm	
Receiver Sensitivity each lane (OMAouter) for TDECQ ＜1.4 dB for 1.4 dB ≤ TDECQ ≤ 3.9 dB	SEN_{OMA}			-6.8 –8.2 + TECQ	dBm	5
Stressed receiver sensitivity (OMAouter), per lane	SRS_{OMA}			-4.3	dBm	6
Receiver Reflectance				-26.0	dB	
LOS Assert	LOSA	-15			dBm	
LOS De-assert	LOSD			-8.9	dBm	
LOS Hysteresis	LOSH	1.5			dB	

Notes:

1. The optical power is launched into SMF.
2. Even if the TDECQ < 1.4 dB for an extinction ratio of ≥ 5 dB or TDECQ < 1.1 dB for an extinction ratio of < 5 dB, the OMAouter (min) must

exceed the minimum value specified here.

3. The receiver shall be able to tolerate, without damage, continuous exposure to an optical input signal having this average power level. The receiver does not have to operate correctly at this input power.
4. Average receive power, each lane (min) is informative and not the principal indicator of signal strength.
5. Receiver sensitivity (OMA_{outer}),each lane (max) is informative and is defined for a transmitter with SECQ up to 3.4 dB
6. Measured with conformance test signal at TP3 using the test pattern PRBS31Q or scrambled idle for stressed receiver sensitivity for the BER= $2.4x10^{-4}$..

IV、Electrical Characteristics

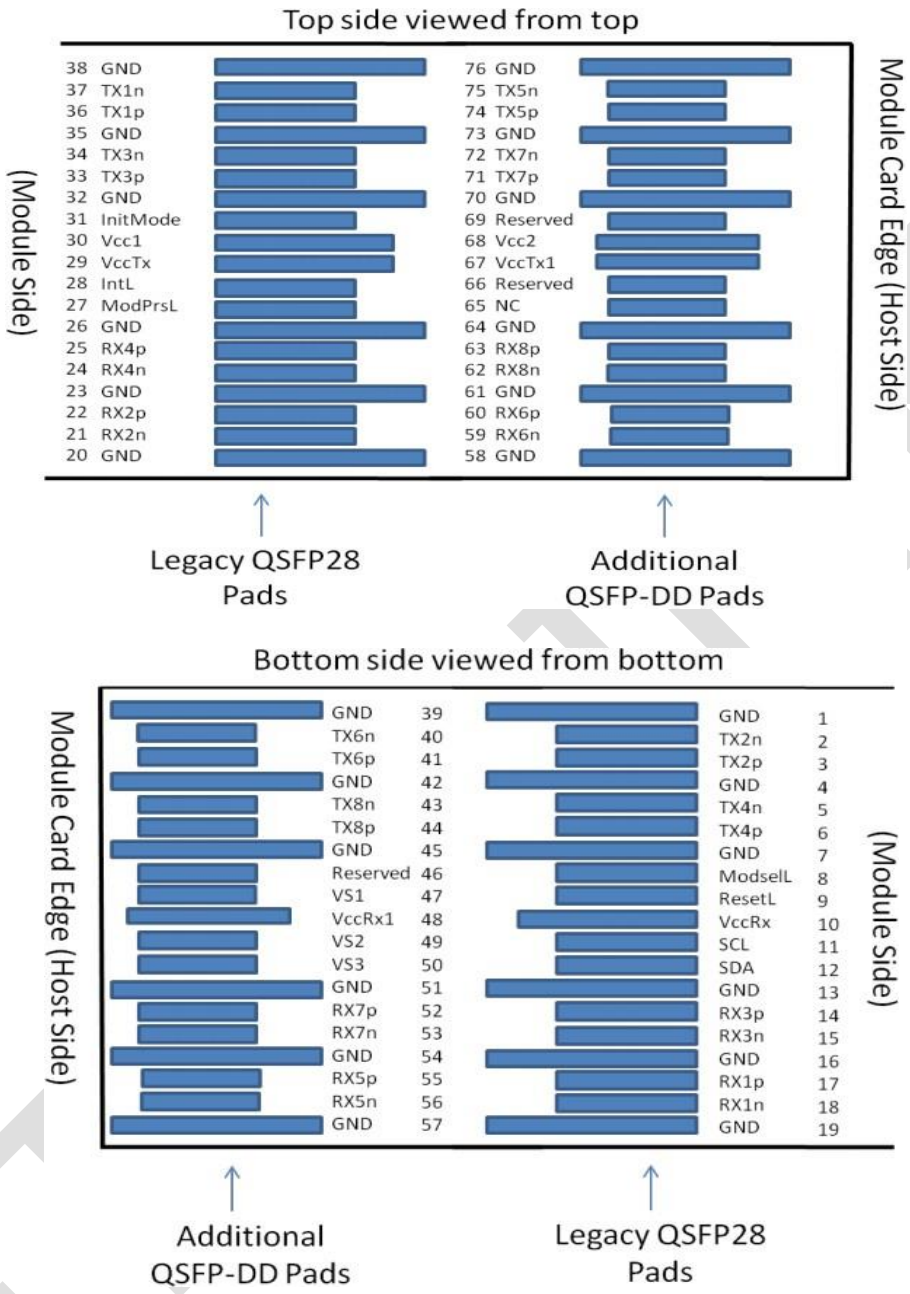
High-Speed Signal: Compliant to 400GAUI-8 (IEEE 802.3bs)
Low-Speed Signal: Compliant to QSFP-DD-Hardware-rev5p2.

Parameter	Symbol	Min.	Typical	Max.	Unit	Notes
Transmitter (Module Input)						
Differential Data Input Amplitude	VIN,P-P	900	-	-	mVpp	
Differential Termination Mismatch		-	-	10	%	
Receiver (Module Output)						
Differential Data Output Amplitude	VOUT,P-P	-	-	900	mVpp	
Differential Termination Mismatch (1MHZ)		-	-	10	%	
Low-speed Electrical Interface						
LPMode, ResetL, ModSelL and ePPS	VIL	-0.3	-	0.8	V	
	VIH	2.0	-	VCC+0.3	V	
ModPrsL	VOL	0	-	0.4	V	
	VIH	ModPrsL can be implemented as a short-circuit to GND on the module				
IntL	VOL	0	-	0.4	V	
	VOH	VCC-0.5	-	VCC+0.3	V	

VI、Digital Diagnostic Monitoring Specifications

Parameter	Unit	Specification
Temperature Monitor absolute error	℃	±3.0
Supply Voltage Monitor absolute error	%	± 5℃
I_bias Monitor absolute error	%	± 10
Received Power (Rx) Monitor absolute error	dB	± 3.0
Transmit Power (Tx) Monitor absolute error	dB	± 3.0

VII、Pin Assignment and Description



PIN	Logic	Symbol	Description	Plug Seq.	Notes
1		GND	Ground	1B	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	3B	
3	CML-I	Tx2p	Transmitter Non-Inverted Data output	3B	
4		GND	Ground	1B	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	3B	
6	CML-I	Tx4p	Transmitter Non-Inverted Data output	3B	
7		GND	Ground	1B	1

8	LVTLL-I	ModSelL	Module Select	3B	
9	LVTLL-I	ResetL	Module Reset	3B	
10		VccRx	+ 3.3V Power Supply Receiver	2B	2
11	LVCMOS-I/O	SCL	2-Wire Serial Interface Clock	3B	
12	LVCMOS-I/O	SDA	2-Wire Serial Interface Data	3B	
13		GND	Ground	1B	
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	3B	
15	CML-O	Rx3n	Receiver Inverted Data Output	3B	
16		GND	Ground	1B	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	3B	
18	CML-O	Rx1n	Receiver Inverted Data Output	3B	
19		GND	Ground	1B	1
20		GND	Ground	1B	1
21	CML-O	Rx2n	Receiver Inverted Data Output	3B	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	3B	
23		GND	Ground	1B	1
24	CML-O	Rx4n	Receiver Inverted Data Output	3B	
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	3B	
26		GND	Ground	1B	1
27	LVTTL-O	ModPrsL	Module Present	3B	
28	LVTTL-O	IntL/RX_LOS	Interrupt/RX_LOS	3B	
29		VccTx	+3.3 V Power Supply transmitter	2B	2
30		Vcc1	+3.3 V Power Supply	2B	2
31	LVTTL-I	LPMode/Tx_DIS	Low Power Mode/Tx Disable	3B	
32		GND	Ground	1B	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	3B	
34	CML-I	Tx3n	Transmitter Inverted Data Input	3B	
35		GND	Ground	1B	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	3B	
37	CML-I	Tx1n	Transmitter Inverted Data Input	3B	
38		GND	Ground	1B	1
39		GND	Ground	1A	
40	CML-I	Tx6n	Transmitter Inverted Data Input	3A	

41	CML-I	Tx6p	Transmitter Non-Inverted Data Input	3A	
42		GND	Ground	1A	1
43	CML-I	Tx8n	Transmitter Inverted Data Input	3A	
44	CML-I	Tx8p	Transmitter Non-Inverted Data Input	3A	
45		GND	Ground	1A	1
46		Reserved	For future use	3A	3
47		VS1	Module Vendor Specific 1	3A	3
48		VccRx1	3.3V Power Supply	2A	2
49		VS2	Module Vendor Specific 2	3A	3
50		VS3	Module Vendor Specific 3	3A	3
51		GND	Ground	1A	1
52	CML-O	Rx7p	Receiver Non-Inverted Data Output	3A	
53	CML-O	Rx7n	Receiver Inverted Data Output	3A	
54		GND	Ground	1A	1
55	CML-O	Rx5p	Receiver Non-Inverted Data Output	3A	
56	CML-O	Rx5n	Receiver Inverted Data Output	3A	
57		GND	Ground	1A	1
58		GND	Ground	1A	1
59	CML-O	Rx6n	Receiver Inverted Data Output	3A	
60	CML-O	Rx6p	Receiver Non-Inverted Data Output	3A	
61		GND	Ground	1A	1
62	CML-O	Rx8n	Receiver Inverted Data Output	3A	
63	CML-O	Rx8p	Receiver Non-Inverted Data Output	3A	
64		GND	Ground	1A	1
65		NC	No Connect	3A	3
66		Reserved	For future use	3A	3
67		VccTx1	3.3V Power Supply	2A	2
68		Vcc2	3.3V Power Supply	2A	2
69		Reserved	For future use	3A	3
70		GND	Ground	1A	1
71	CML-I	Tx7p	Transmitter Non-Inverted Data Input	3A	
72	CML-I	Tx7n	Transmitter Inverted Data Input	3A	
73		GND	Ground	1A	1
74	CML-I	Tx5p	Transmitter Non-Inverted Data Input	3A	

75	CML-I	Tx5n	Transmitter Inverted Data Input	3A	
76		GND	Ground	1A	1

Notes:

1. QSFP-DD uses common ground (GND)for all signals and supply (power). All are common within the QSFP-DD module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane.
2. VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 shall be applied concurrently. Requirements defined for the host side of the Host Card Edge Connector are listed in Table 6，as per QSFP-DD Hardware Specification V4.0. VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 may be internally connected within the module in any combination. The connector Vcc pins are each rated for a maximum current of 1000 mA.
3. All Vendor Specific, Reserved and No Connect pins may be terminated with 50 ohms to ground on the host. Pin65 (No Connect) shall be left unconnected within the module. Vendor specific and Reserved Pins shall have an impedance to GND that is greater than 10 kOhms and less than 100 pF.
4. Plug Sequence specifies the mating sequence of the host connector and module. The sequence is 1A, 2A, 3A, 1B, 2B, 3B. (see Figure 2 for pad locations) Contact sequence A will make, then break contact with additional QSFP-DD pads. Sequence 1A, 1B will then occur simultaneously, followed by 2A, 2B, followed by 3A,3B.

VIII、Laser Safety

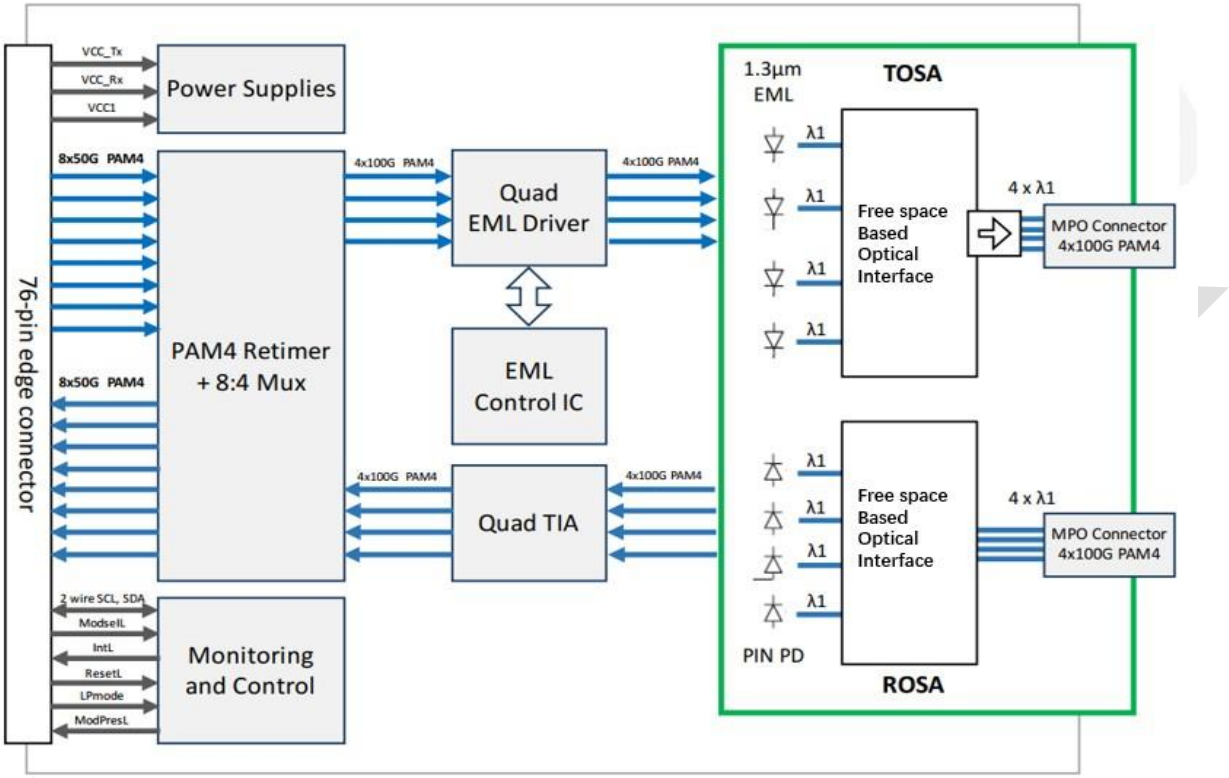
This is a Class 1 Laser Product according to EN 60825-1:2014. This product complies with 21 CFR 1040.10 and 1040.11 except for deviations pursuant to Laser Notice No. 50, dated (June 24, 2007).

Caution: Use of controls or adjustments or performance of procedures other than those specified herein may result in hazardous radiation exposure.

IX、ESD

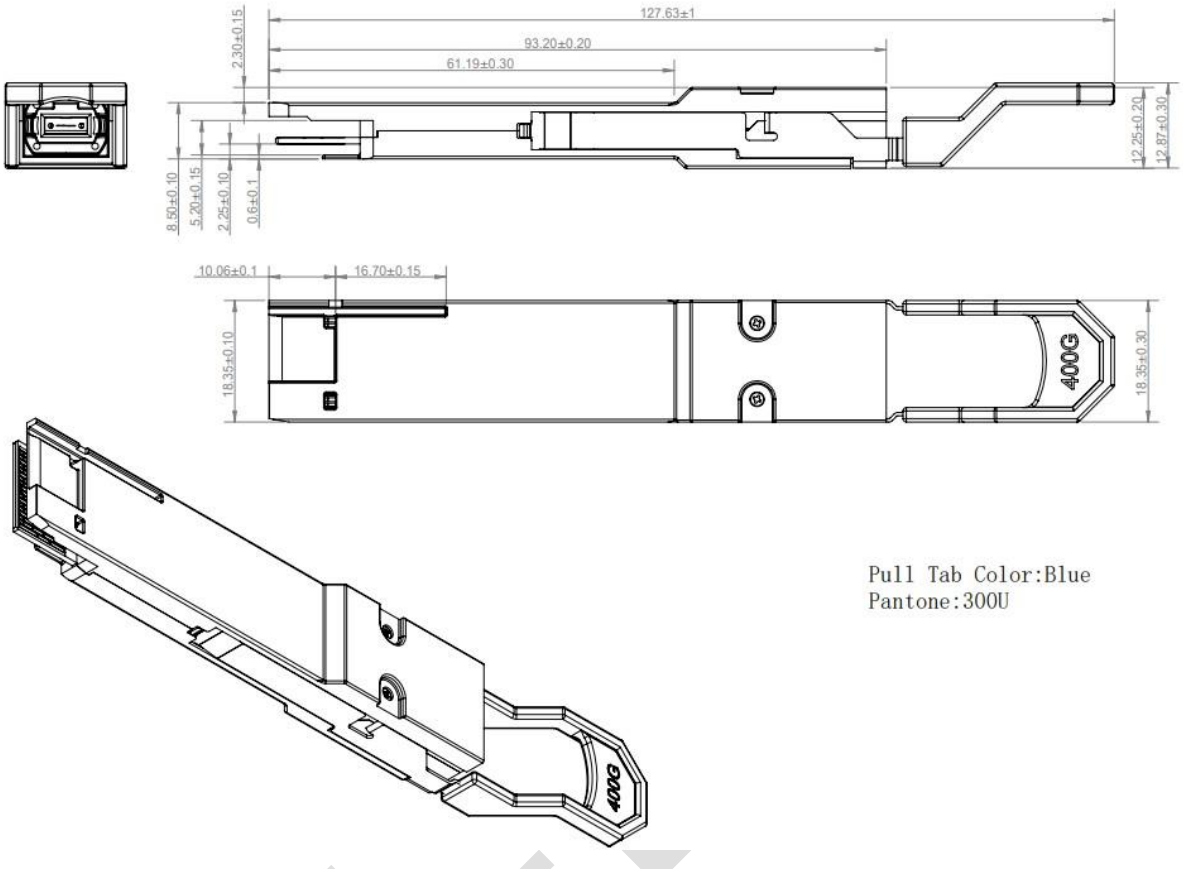
This transceiver is specified as ESD threshold 1KV for high speed data pins and 2KV for all others electrical input pins, tested per MIL-STD-883, Method 3015.4 /JESD22-A114-A (HBM). However, normal ESD precautions are still required during the handling of this module. This transceiver is shipped in ESD protective packaging. It should be removed from the packaging and handled only in an ESD protected environment.

X、Module Block Diagram



XI、Mechanical Dimensions

Unit: mm



XII、Revision History

Version No.	Date	Description
1.0	Aug 18 2023	Preliminary datasheet

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