

## **EQD200-SR8**

### **200G QSFP28-DD SR8 100M Optical transceiver**

#### **PRODUCT FEATURES**

- **Up to 25.78Gbps data rate per channel by NRZ modulation**
- **Support 200GAUI-8 electrical interface**
- **Integrated 850nm VCSEL array and PD array**
- **Single MPO16 connector receptacle optical interface compliant**
- **DDM function implemented**
- **Case temperature range: 0°C ~ +70°C**
- **Hot-pluggable QSFP-DD form factor**
- **Maximum power consumption <4W**
- **Single +3.3V power supply**
- **Reach up to 70m on MMF(OM3)**
- **Reach up to 100m on MMF(OM4)**
- **Compliant with ROHS2.0**

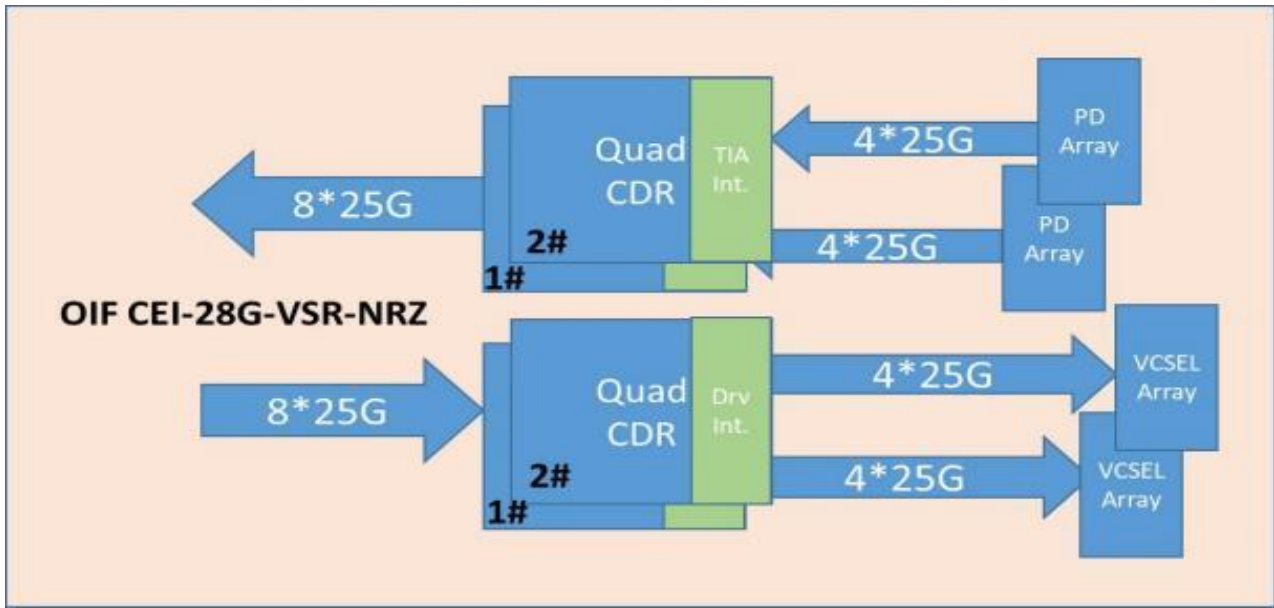
#### **APPLICATIONS**

- **Data centers and Cloud Networks**
- **200G Interconnect Requirements**

#### **DESCRIPTIONS**

The QSFP28-DD 200G SR8 Transceiver is designed to transmit and receive serial optical data links up to 8 x 25.78Gbps data rate by NRZ modulation format over multi-mode fiber.

## Module Block Diagram



## Ordering Information

Part No.	Data Rate(optical)	Laser	Fiber Type	Distance	Optical Interface	Temp	DDMI	Latch Color
EQP200-SR8	200G	VCSEL	MMF	100M	MPO16	0°C~ +70°C	Y	

## Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit	Note
Supply Voltage	V	0	3.6	V	
Storage Temperature	T <sub>STG</sub>	-40	85	C	Ambient
Relative Humidity	RH	5	85	%	

## Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit	Note
operating case Temperature	Top	0	-	70	C	
Power Supply Voltage	V <sub>cc</sub>	3.14	3.3	3.46	V	
Power Supply Current	I <sub>cc</sub>	-		1210	mA	
Power Consumption				4	W	

## Electrical Characteristics

Parameter	Symbol	Min	Typical	Max	Unit
Differential input impedance	Zin	90	100	110	ohm
Differential Output impedance	Zout	90	100	110	ohm
Differential input voltage amplitude aAmplitude	$\Delta V_{in}$	300		1100	mVp-p
Differential output voltage amplitude	$\Delta V_{out}$	500		800	mVp-p
Skew	Sw			300	ps
Bit Error Rate	BER			5E-5	
Input Logic Level High	VIH	2.0		VCC	V
Input Logic Level Low	VIL	0		0.8	V
Output Logic Level High	VOH	VCC-0.5		VCC	V
Output Logic Level Low	VOL	0		0.4	V

Note:

1. BER=5E-5; PRBS 2<sup>31</sup>-1@25.78125Gbps. Pre-FEC
2. Differential input voltage amplitude is measured between TxnP and TxnN.
3. Differential output voltage amplitude is measured between RxnP and RxnN.

## Optical and Characteristics

Parameter	Min	Typical	Max	Unit	Note
<b>Transmitter</b>					
Signaling rate, each lane	25.78125±100ppm			Gb/s	
Lane Wavelength Range	840		860	nm	
Modulation Format	NRZ				
Average Optical Power per lane	-8.4		2.4	dBm	1
RMS Spectral width			0.6	nm	
Optical Modulation Amplitude (OMA), each lane	-6.4		3	dBm	
Average launch power of OFF transmitter, each lane			-30	dBm	
Launch Power in OMA minus TDEC, each lane	-7.3			dBm	
Transmitter and Dispersion Eye Closure, each lane			4.3	dB	
Extinction Ratio	2				
Data Input Differential Peak-to Peak Voltage Swing	20		950	mVpp	2

## Optical Communications Products Alliance

LOS Assert Threshold	120			mVpp	3
Optical Return Loss Tolerance			12	dB	
Transmitter Eye mask definition{X1,X2,X2,Y1,Y2,Y3}	{0.3,0.38,0.45,0.35,0.41,0.5}				
<b>Receiver</b>					

Signaling rate, each lane	25.78125±100ppm			Gb/s	
Lane Wavelength Range	840		860	nm	
Modulation Format	NRZ				
Damage Threshold	3.4			dBm	
Average Receive Power, each lane	-10.3		2.4	dBm	
Receiver Power, each lane (OMA)			3.0	dBm	4
Receiver Reflectance			-12.0	dB	
Stressed Receiver Sensitivity(OMA),each lane			-5.2	dBm	5
Data Output Differential Peak-to Peak Voltage Swing, each lane	300		800	mVpp	
RX_Los_Assert Min/Max	-30.0			dBm	
RX_Los_De-ASSERT Min/Max			-12.0	dBm	
RX_Los_Hysteresis	0.5			dBm	
Stresssd Receiver Eye Mask Definition{X1,X2,X2,Y1,Y2,Y3}	{0.28,0.5,0.5,0.33,0.33,0.4}				

## Notes:

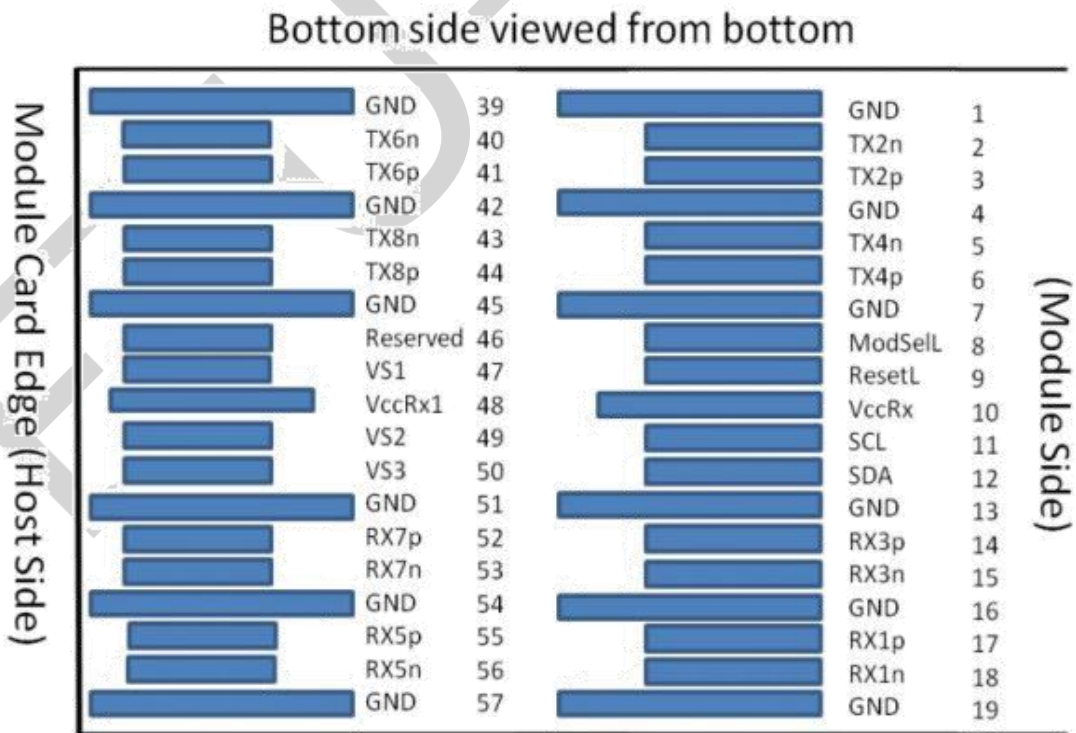
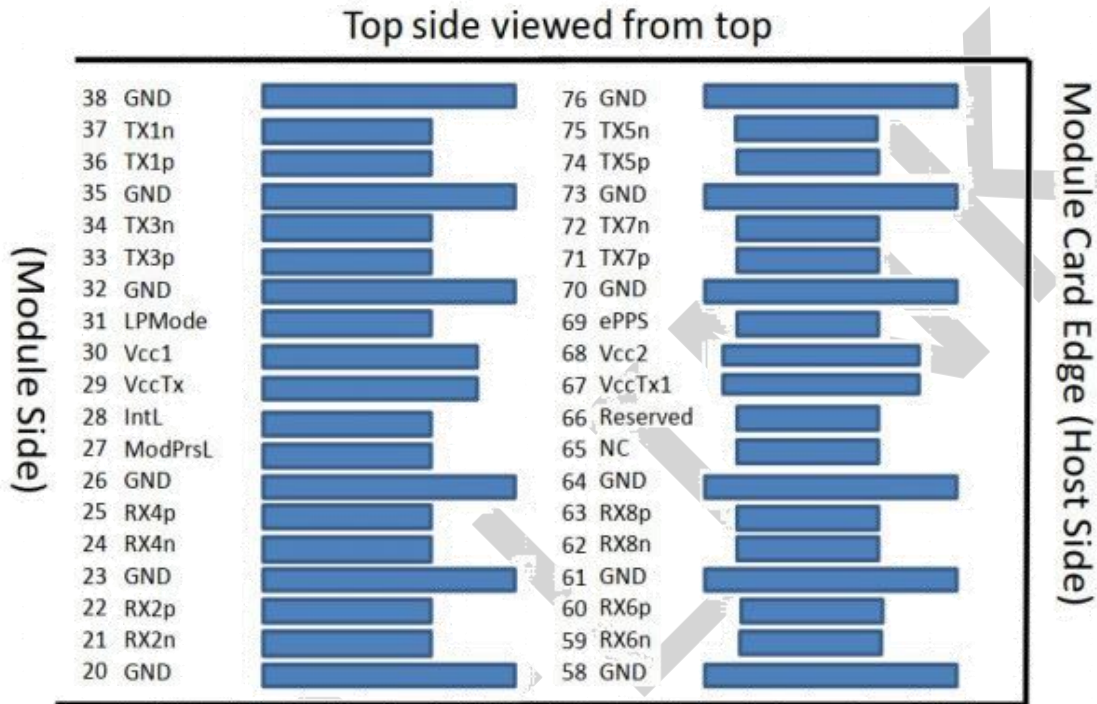
1. Even if the TDP<0.9dB,the OMA(min) most exceed this value
2. AC coupled internally.
3. Tx Data Input Differential Peak-to-Peak Voltage Swing
4. Measured with 25.78125-Gbps of PRBS-31 at 5x10<sup>-5</sup> BER.
5. AC coupled with 100ohm differential output impedance.

## Digital Diagnostics

Parameter	Range	Accuracy	Unit	Calibration
Temperature	0 to 70	±3	°C	Internal
Voltage	0 to VCC	3%	V	Internal
Tx Bias Current (Each Lane)	0 to 10	10%	mA	Internal
Tx Output Power (Each Lane)	-8.4 to +2.4	±3	dB	Internal

Parameter	Range	Accuracy	Unit	Calibration
Rx Receive Power (Each Lane)	-10.3 to +3.4	±3	dB	Internal

Pin Diagram

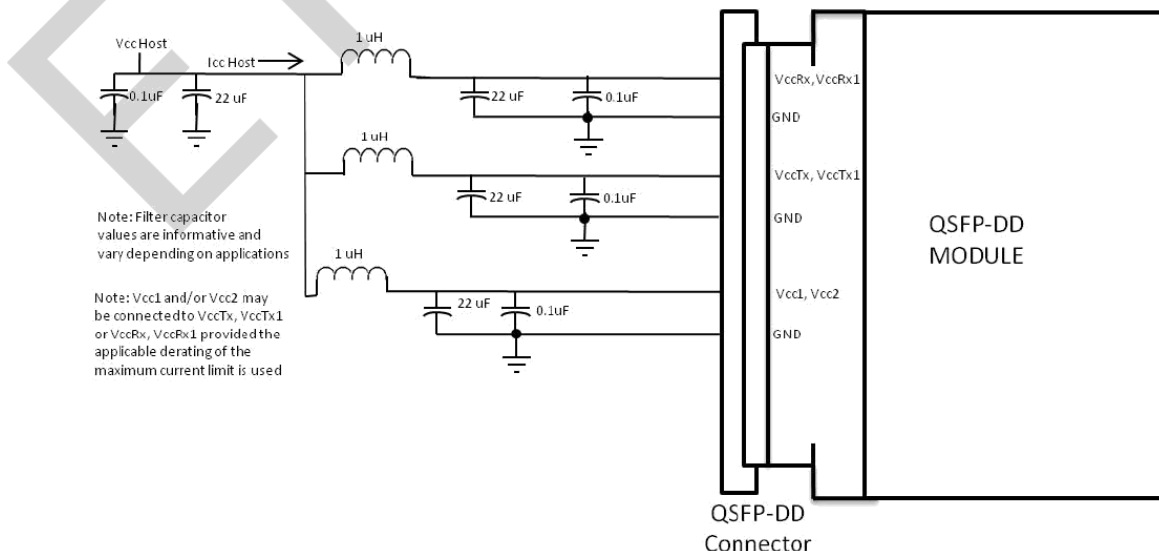


## Pin Definitions

Pin #	Logic	Symbol	Definition	Pin #	Logic	Symbol	Definition
1		GND	Ground	39		GND	Ground
2	CML-I	Tx2n	Transmitter Inverted Data Input	40	CML-I	Tx6n	Transmitter Inverted Data Input
3	CML-I	Tx2p	Transmitter Non-inverted Data Input	41	CML-I	Tx6p	Transmitter Non-inverted Data Input
4		GND	Ground	42		GND	Ground
5	CML-I	Tx4n	Transmitter Inverted Data Input	43	CML-I	Tx8n	Transmitter Inverted Data Input
6	CML-I	Tx4p	Transmitter Non-inverted Data Input	44	CML-I	Tx8p	Transmitter Non-inverted Data Input
7		GND	Ground	45		GND	Ground
8	LVTTL-I	ModSelL	Module Select	46		Reserve d	
9	LVTTL-I	ResetL	Module Reset	47		VS1	Module Vendor Specific 1
10		VccRx	+3.3V Power Supply Receiver	48		VccRx1	3.3V Power Supply
11	LVCMS-I/O	SCL	2-wire serial interface clock	49		VS2	Module Vendor Specific 2
12	LVCMS-I/O	SDA	2-wire serial interface data	50		VS3	Module Vendor Specific 3
13		GND	Ground	51		GND	Ground
14	CML-O	Rx3p	Receiver Non-inverted Data Output	52	CML-O	Rx7p	Receiver Non-inverted Data Output
15	CML-O	Rx3n	Receiver Inverted Data Output	53	CML-O	Rx7n	Receiver Inverted Data Output
16		GND	Ground	54		GND	Ground
17	CML-O	Rx1p	Receiver Non-inverted Data Output	55	CML-O	Rx5p	Receiver Non-inverted Data Output
18	CML-O	Rx1n	Receiver Inverted Data Output	56	CML-O	Rx5n	Receiver Inverted Data Output
19		GND	Ground	57		GND	Ground
20		GND	Ground	58		GND	Ground
21	CML-O	Rx2n	Receiver Inverted Data Output	59	CML-O	Rx6n	Receiver Inverted Data Output
22	CML-O	Rx2p	Receiver Non-inverted Data Output	60	CML-O	Rx6p	Receiver Non-inverted Data Output
23		GND	Ground	61		GND	Ground

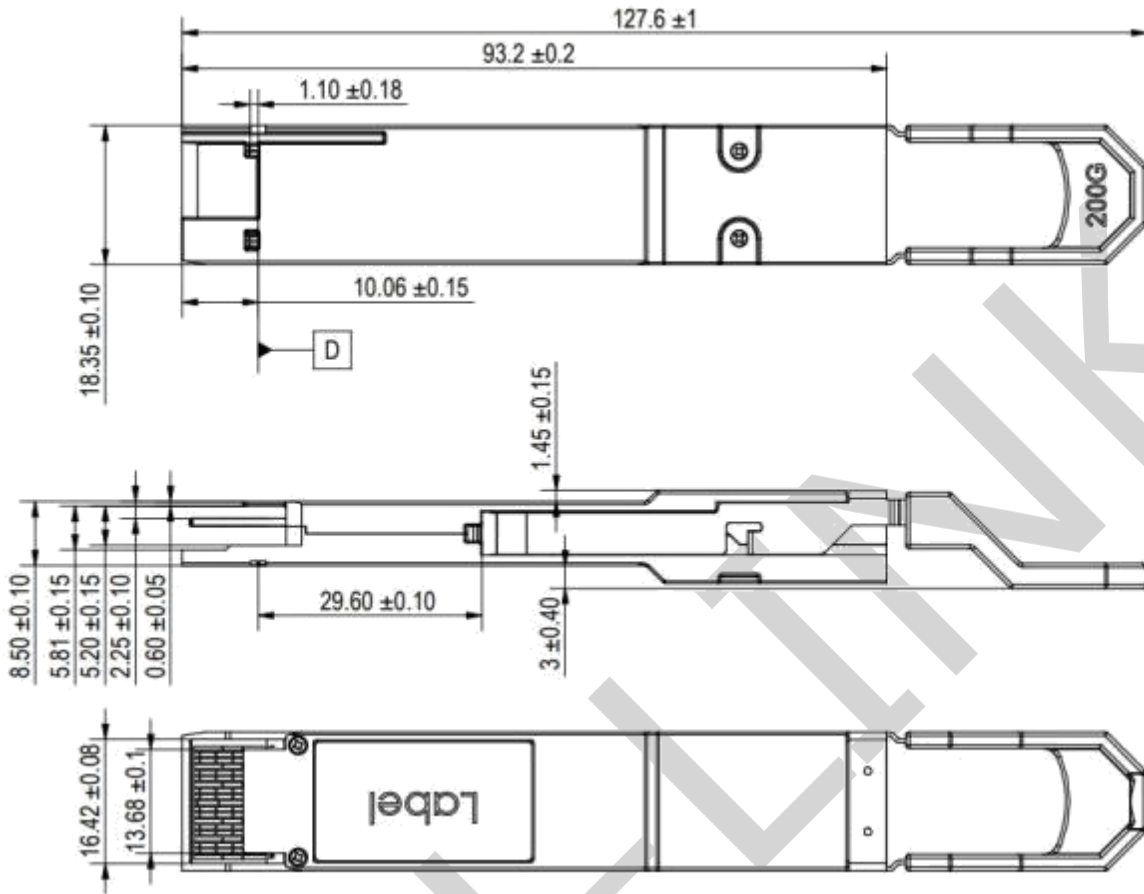
Pin #	Logic	Symbol	Definition	Pin #	Logic	Symbol	Definition
24	CML-O	Rx4n	Receiver Inverted Data Output	62	CML-O	Rx8n	Receiver Inverted Data Output
25	CML-O	Rx4p	Receiver Non-inverted Data Output	63	CML-O	Rx8p	Receiver Non-inverted Data Output
26		GND	Ground	64		GND	Ground
27	LVTTL-O	ModPrsL	Module Present	65		NC	Not connected
28	LVTTL-O	IntL	Interrupt	66		Reserved	
29		VccTx	+3.3V Power Supply Transmitter	67		VccTx1	3.3V Power Supply
30		Vcc1	+3.3V Power Supply	68		Vcc2	3.3V Power Supply
31	LVTTL-I	InitMode	Initialization mode	69		Reserved	
32		GND	Ground	70		GND	Ground
33	CML-I	Tx3p	Transmitter Non-inverted Data Input	71	CML-I	Tx7p	Transmitter Non-inverted Data Input
34	CML-I	Tx3n	Transmitter Inverted Data Input	72	CML-I	Tx7n	Transmitter Inverted Data Input
35		GND	Ground	73		GND	Ground
36	CML-I	Tx1p	Transmitter Non-inverted Data Input	74	CML-I	Tx5p	Transmitter Non-inverted Data Input
37	CML-I	Tx1n	Transmitter Inverted Data Input	75	CML-I	Tx5n	Transmitter Inverted Data Input
38		GND	Ground	76		GND	Ground

## Recommended Interface Circuit



## Mechanical Diagram

Compatible with the QSFP28-DD Type 2 Specification for pluggable form factor modules.



## Revision History

Version No.	Date	Description
1.0	Aug 18, 2022	Preliminary datasheet
2.0	Sep 20, 2024	Format change

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