

EQSX-CVR

40Gbps QSFP+ to 10G SFP+ Converter

PRODUCT FEATURES

- Trouble-free installation and network bring-up
- Compliant to industry standards: SFF-8665/ SFF-8432
- Precision process control for minimization of pair-to-pair skew
- 1 independent duplex channels operating at 25Gbps and 10Gbps
- Good EMI performance
- 100ohm differential impedance system
- Operating case temperature: -40 to 85°C
- Low insertion loss, Low crosstalk
- RoHS compliant

APPLICATIONS

- Low EMI radiation Switches, servers and routers
- Telecommunication and wireless infrastructure
- Test and measurement equipment
- Networked storage systems
- Data Center networks
- Storage area networks



DESCRIPTIONS

The QSFP form factor to SFP form factor Adapter (QTSA) Module offers 25Gigabit or 10 Gigabit Ethernet connectivity for Quad Small Form-Factor Pluggable (QSFP)-only platforms. It allows smooth and cost-effective migration to 100 Gigabit Ethernet or 40 Gigabit Ethernet by providing an option to use lower-speed Small Form-Factor Pluggable (SFP) or Enhanced Small Form-Factor Pluggable (SFP+) modules in empty QSFP ports or when the other end of the network is running at lower speeds.

Ordering Information

Part No.	Description
EQSX-CVR	40Gbps QSFP+ to 10G SFP+ Converter

A list of SFP+ or SFP28 transceiver modules that can be plugged into the QTSA module is provided in Table 1.

Item	Product name	Product description
1	SFP+ SR	SFP+ SR Module for Multimode Fiber
2	SFP+ LR	SFP+ LR Module for Single-Mode Fiber
3	SFP28 SR	25GBASE-SR SFP28 Module for Multimode Fiber
4	SFP28 LR	25GBASE-LR SFP28 Module for Single-Mode Fiber
5	AOC	SFP28 and SFP+ AOC Optical Cables
6	DAC	SFP28 and SFP+ Copper Cables (1-m to 5-m lengths)

Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
Storage Temperature	Ts	-40	85	°C
Case Operating Temperature	Top	-40	85	°C
Relative Humidity (non-condensation)	RH	5	95	%
Supply Voltage	Vcc	-0.5	3.6	V

Input Voltage	V _{in}	-0.5	V _{CC} +0.5	V
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Recommended Operating Conditions

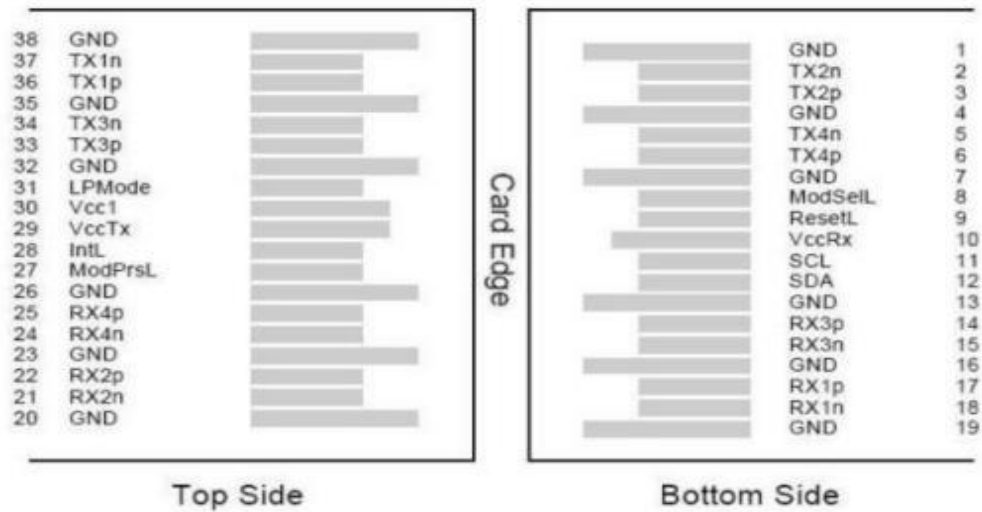
Parameter	Symbol	Min	Max	Unit
Operating Case Temperature	T _{op}	-40	85	°C
Relative Humidity(non- condensation)	RH	5	85	%
Power Supply Voltage	V _{cc}	3.135	3.465	V

Electrical Characteristics

Parameter	Symbol	Min	Max	Unit
Host 2-wire V _{cc} voltage	V _{cc_Host_2 w}	3.14	3.46	V
SCL and SDA Voltage ^[1]	V _{OL}	0.0	0.40	V
	V _{OH}	V _{cc_Host_2w} - 0.5	V _{cc_Host_2w} + 0.3	V
	V _{IL}	-0.3	V _{ccT} *0.3	V
	V _{IH}	V _{ccT} *0.7	V _{ccT} +0.5	V
Input current on the SCL and SDA contacts	I _l	-10	10	mA

Pin Diagram

QSFP+ Transceiver Pad Layout, host PCB QSFP+ Pinout, and PIN Descriptions are as follows:



QSFP+ Transceiver Electrical Pad Pinout

Pin Definitions

Pin#	Name	Logic	Description	Power Seq.	Note
1	GND		Ground	1st	1
2	Tx2n	CML-I	Transmitter Inverted Data Input	3rd	
3	Tx2p	CML-I	Transmitter Non-Inverted Data output	3rd	
4	GND		Ground	1st	1
5	Tx4n	CML-I	Transmitter Inverted Data Input	3rd	
6	Tx4p	CML-I	Transmitter Non-Inverted Data output	3rd	
7	GND		Ground	1st	1
8	ModSelL	LVTLL-I	Module Select	3rd	
9	ResetL	LVTLL-I	Module Reset	3rd	
10	VccRx		+3.3V Power Supply Receiver	2nd	2
11	SCL	LVC MOS-I/O	2-Wire Serial Interface Clock	3rd	
12	SDA	LVC MOS-I/O	2-Wire Serial Interface Data	3rd	
13	GND		Ground	1st	1

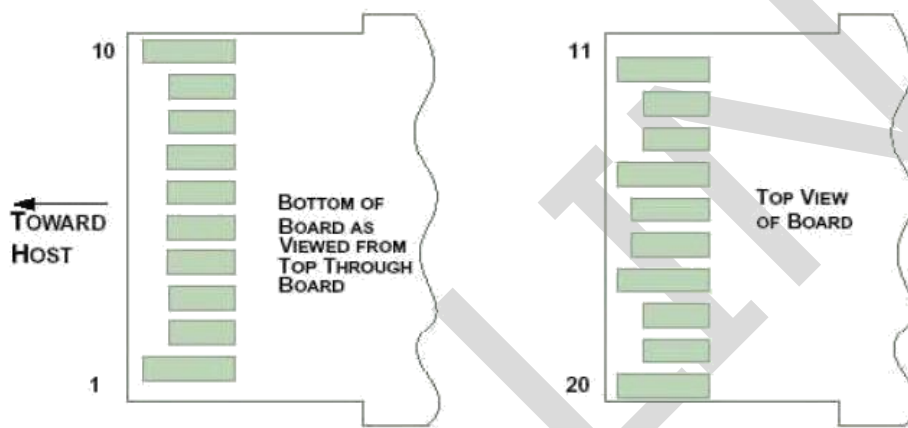
14	Rx3p	CML-O	Receiver Non-Inverted Data Output	3rd	
15	Rx3n	CML-O	Receiver Inverted Data Output	3rd	
16	GND		Ground	1st	1
17	Rx1p	CML-O	Receiver Non-Inverted Data Output	3rd	
18	Rx1n	CML-O	Receiver Inverted Data Output	3rd	
19	GND		Ground	1st	1
20	GND		Ground	1st	1
21	Rx2n	CML-O	Receiver Inverted Data Output	3rd	
22	Rx2p	CML-O	Receiver Non-Inverted Data Output	3rd	
23	GND		Ground	1st	1
24	Rx4n	CML-O	Receiver Inverted Data Output	3rd	
25	Rx4p	CML-O	Receiver Non-Inverted Data Output	3rd	
26	GND		Ground	1st	1
27	ModPrsL	LVTTL-O	Module Present	3rd	
28	IntL	LVTTL-O	Interrupt	3rd	
29	VccTx		+3.3 V Power Supply transmitter	2nd	2
30	Vcc1		+3.3 V Power Supply	2nd	2
31	LPMODE	LVTTL-I	Low Power Mode	3rd	
32	GND		Ground	1st	1
33	Tx3p	CML-I	Transmitter Non-Inverted Data Input	3rd	
34	Tx3n	CML-I	Transmitter Inverted Data Output	3rd	
35	GND		Ground	1st	1
36	Tx1p	CML-I	Transmitter Non-Inverted Data Input	3rd	
37	Tx1n	CML-I	Transmitter Inverted Data Output	3rd	

38	GND		Ground	1st	1
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Notes:

1. GND is the symbol for signal and supply (power) common for the QSFP+ module. All are common within the QSFP+ module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane.
2. Vcc Rx, Vcc1 and Vcc Tx are the receiver and transmitter power supplies and shall be applied concurrently. Vcc Rx, Vcc1 and Vcc Tx may be internally connected within the QSFP+ transceiver module in any combination. The connector pins are each rated for a maximum current of 500 mA.

SFP28 Host board Connector Pinout



Pin Definitions

Pin	Logic	Symbol	Name/Description	Note
1		VeeT	Module Transmitter Ground	1
2	LVTTL-O	Tx_Fault	Transmitter Fault	2
3	LVTTL-I	Tx_Disable	Transmitter Disable	3
4	LVTTL-I/O	SDA	MOD-DEF2 2-wire serial interface data line	4
5	LVTTL-I/O	SCL	MOD-DEF1 2-wire serial interface clock line	4
6		Mod_Abs	Module Absent	5
7	LVTTL-I	RS0	Rate Select Zero	
8	LVTTL-O	Rx_LOS	Module Receiver Loss of Signal	2
9	LVTTL-I	RS1	Rate Select One	
10		VeeR	Module Receiver Ground	1
11		VeeR	Module Receiver Ground	1
12	CML-O	RD-	Receiver Inverted Data Output	
13	CML-O	RD+	Receiver Non-Inverted Data Output	
14		VeeR	Module Receiver Ground	1
15		VccR	Module Receiver 3.3V Supply	

16		VccT	Module Transmitter 3.3V Supply	
17		VeeT	Module Transmitter Ground	1
18	CML-I	TD+	Transmitter Non-Inverted Data Input	
19	CML-I	TD-	Transmitter Inverted Data Input	
20		VeeT	Module Transmitter Ground	1

Notes:

1. The module signal grounds, VeeR and VeeT, shall be isolated from the module case.
2. This is an open collector/drain output and shall be pulled up with 4.7-10k to Vcc_Host on the host board. Pull ups can be connected to multiple power supplies, however the host board design shall ensure that no module has voltage exceeding module VccT/R + 0.5 V.
3. This is an open collector/drain input and shall be pulled up with 4.7-10k to VccT in the module.
4. See 2-wire electrical specifications.
5. This shall be pulled up with 4.7-10k to Vcc_Host on the host board

Recommended Interface Circuit

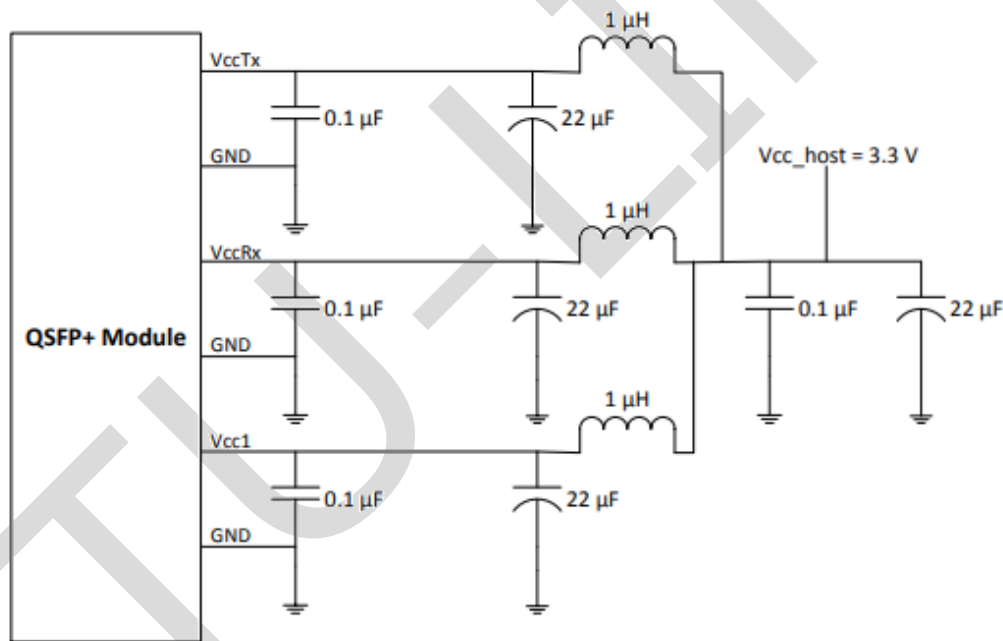
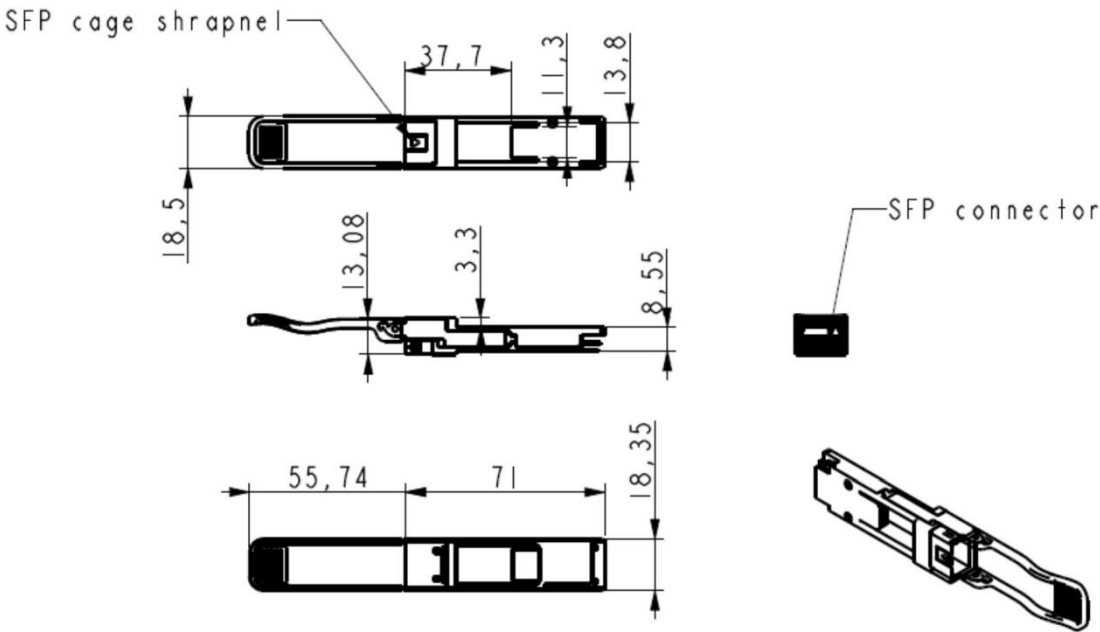


FIGURE 5-4 RECOMMENDED HOST BOARD POWER SUPPLY FILTERING

Mechanical Diagram

Figure shows the package dimensions of the module. The module is designed to be compliant with QSFP+ MSA specification. Package dimensions are specified in SFF-8436.



Revision History

Version No.	Date	Description
1.0	February 18, 2019	Preliminary datasheet
2.0	July 15,2024	Format change
2.1	anuary 14th, 2026	Update the temperature parameters of the module

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